Gryphon100
User's Manual

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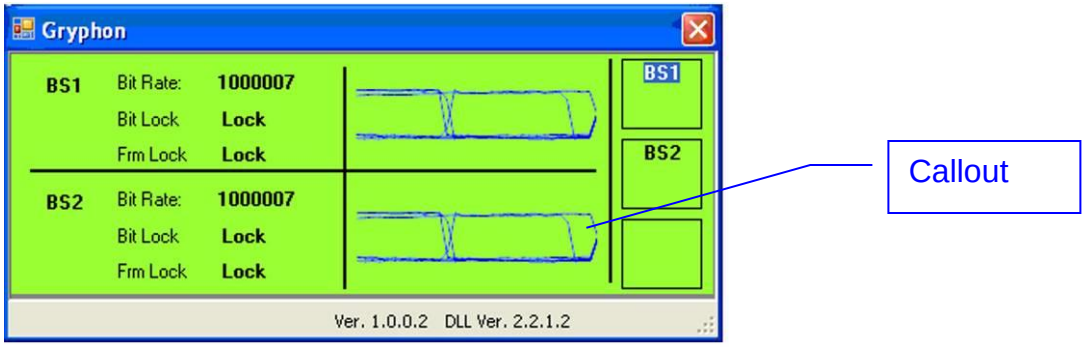
About this Manual

Conventions Used

Screen Instructions

Many Gryphon100 screens are shown throughout the manual. The screens are shown as Windows images of the LCD Display on the Gryphon. There are callouts on the left and right sides and lines pointing to specific features. The callouts indicate features and controls that are normally not explained in the step by step instructions for the screen.



Caution Notes

The caution sign is used throughout the manual to help clarify operational procedures and result from operations that may not be intuitively clear. The intent is to save the user time and eliminate frustration during the setup and operation of the Gryphon100 system.

Special Features

Special features are advanced options that the Ulyssix engineers have developed to help customers solve complex problems, minimize setup problems, help in troubleshooting and bring PCM equipment to the forefront in technology. Special features are indicated throughout the manual by the light bulb icon.

Menus Paths

Menus are a set of hierarchal commands used to open windows or perform commands. Using menus usually consist of a multi-step process of selecting the top-level menu, then its sub-menu and possibly sub-sub-menus. The multi-step menu process is used throughout the Gryphon100 software and throughout this manual and is referred to as the menu path. All references to menu paths are indicated by ***Bold Italic*** text and each step is separated by the back-slash character "****".

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Chapter 1 Introduction

1.1 Overview

The Gryphon100 Multiple Bit Synchronizer/Frame Synchronizer System is a fully integrated chassis solution that may be configured with either two or four bit synchronizers and frame synchronizers with an internal an IRIG time code reader. The Gryphon100 system utilizes the Ulyssix TarsusHS-02 Dual Bit Synchronizer/Frame Synchronizer w/ IRIG time code reader product which is a state-of-the-art Digital Signal Processing (DSP) based PCM processor board. The chassis is a 2U rack-mount system containing a LCD graphic display and integrated keypad with an advanced computer board running an embedded operating system.

The Gryphon100 archives frame synced data from each channel to an external memory drive via the USB ports. The internal IRIG time code reader time stamps the archived data at the beginning of each minor frame for enhanced post-processing analysis.

The Gryphon100 system can be controlled via integrated keypad or via RS232 or ethernet connection to a host computer. The Gryphon100's main graphic display allows for easy viewing of the bit sync lock and bit rate indicators for all the bit syncs per chassis. There are also bright LEDs for to indicate Bit Lock, Frame Lock and Sub Frame Lock for all channels contained in the chassis. The graphical indicators for the bit synchronizers are synchronized eye diagrams and input digital oscilloscopes.

All firmware upgrades to the internal TarsusHS-02 board is done via USB ports using proprietary Ulyssix utility which is included with the Gryphon100 system.

Bit Synchronizer Features:
• Full Bit Sync design using all DSP filter algorithms in FPGA technology for maximum performance capability.
• Accepts IRIG PCM code types including: NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S
• Bit Sync programmable input rates from 1 bps up to 32 Mbps for NRZ-L/M/S, RNRZ-L, RZ and 1 bps to 16 Mbps for other code types
• Internal IRIG time code reader for time codes A, B, G, and NASA36
• Less than 1 dB theoretical bit sync BER performance
• PCM encoder output capability for IRIG code types
• Second PCM encoder output has external selectable input for use with decryptor interfaces

Frame Synchronizer and System Features
• Supports all IRIG Class II 16 to 33-bit frame synchronizer patterns
• User programmable sync search/check/lock output display strategies
• Minor frame lengths up to 2^{24} bits with up to 1024 sub frames
• Programmable number of frame sync bit slips and allowable sync bit errors
• User friendly setup using face mounted keypad or through RS232 / Ethernet connection to computer running Windows
• Fully integrated 2U rackmount chassis solution including display and keypad

Specifications

Bit Synchronizer Input Specifications

• Number of Bit Syncs	Two or four fully independent inputs per bit sync
• Input Source	Single ended or differential inputs, per bit sync
• Input Data Rate	Bit Sync programmable input tunable rates from 1 bps to 32 Mbps for NRZ-L/M/S, RNRZ-L and 1 bps to 16 Mbps for the other code types (optional versions)
• Input Impedance	Hi-Z/75Ω/50Ω, single ended input, program selectable
• IRIG Time Code Reader	Accepts IRIG time codes A, B, G and NASA36
• Maximum Safe Input	± 35 VDC
• Input Signal Level	75 mVp-p to 10 Vp-p
• DC Input Level	+/- 5 VDC
• Input PCM Code Types Modes	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S program selectable (consult factory for other code types)
• Derandomizer Input	RNRZ 11/15, forward/reverse, program selectable
• Input Polarity	Normal or inverted, program selectable

Bit Synchronizer Data Specifications

• Loop Bandwidth	0.05% to 3.0%, depending on the programmed bit rate
• Data Acquisition Rate	0.01% to 8.0% depending on the programmed bit rate
• Data Tracking Range	+/-5 times of the programmed loop bandwidth
• Bit Error Probability	Less than 1 dB theoretical bit sync BER performance

Bit Synchronizer Output Specifications

• Number of Outputs	2 per bit sync with independent PCM code encoders
• Clock Output	0°, 90°, 180°, 270°, program selectable per output
• Output Signal Levels	TTL Level driven and RS-422 differential
• PCM Encoder Output	TTL Level driven and RS-422 differential
• PCM Encoder Code Types	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, or RNRZ 11/15, program selectable
• PCM Encoder 2 Input Selection	Internal Bit Sync or excepts an external NRZ-L input signal
• Output Polarity	Normal or inverted, program selectable

Frame Synchronizer Specifications

• Input Data Rate	32 Mbps for NRZ-L/M/S, RNRZ-L and 1 bps to 16 Mbps for the other code types
• Input Signals	Direct from the internal Bit Sync or NRZ-L data and clock input
• Minor Frame Length	Up to 16,777,216
• Major Frame Length	1 to 1024 minor frames per major frame
• Frame Sync Pattern	16 to 33 bits
• Frame Sync Strategy	Search-Check-Lock, programmable counts per state

• Sub Frame Sync	FCC or SFID
• Sync Error Tolerance	0 to 31 bits, program selectable
• Sync Slip Window	0 to 9999 bits, program selectable
• Frame Sync Archive	Archive each stream to external memory via USB port

System Specifications

• Processing	Single Board Processor with minimum 32 GB Flash Drive (no storage capability)
• Memory	8 GB minimum RAM
• Operating System	Custom Ulyssix operating system with TCP/IP, USB and RS232 Interfaces
• Display	240 x 64 Graphic LCD Display
• Input	Integrated 24 button keypad
• Dimensions	2U rackmount 19” x 3.5” x 20”
• Ethernet	10/100/1000 RJ45 Ethernet with TCP/IP
• Power	300-Watt ATX power supply, 100 - 240 VAC Full Range
• Temperature Range	Operating: 0°C to 50°C Storage: -20°C to 60°C

Ordering Information

• Gryphon102	1 Tarsus3-02 Dual Bit Sync/Frame Sync card integrated in the 2U rackmount chassis.
• Gryphon104	2 Tarsus3-02 Dual Bit Sync/Frame Sync card integrated in the 2U rackmount chassis.

Warranty

Ulyssix Technologies, Inc. warrants its products to be free from defects in material and workmanship, under normal use and service, for one year from the date of shipment to the original purchaser. The equipment must be returned transportation prepaid to the factory, and if found to be defective, at the Company’s option, will be repaired or replaced free of charge and returned transportation prepaid. If inspection by Ulyssix does not disclose any defect in material or workmanship, Ulyssix standard repair service charge will apply. This warranty does not extend to any products that have been subject to misuse, negligence, modifications or abnormal operating conditions or cover expendable items such as lamps, batteries, fuses, etc. Customer furnished equipment and hardware purchased for resale included in systems are covered by the original manufacturer’s warranty. Ulyssix makes no express or implied warranties beyond those described herein, and in no event will Ulyssix be responsible for consequential damages of any nature arising out of or connected with the use of its products.

Repair Service Charges

Please call the Ulyssix Customer Service Department at 301-846-4800 for a quotation, return authorization number, and shipping information. All units repaired will be warranted for 90 days from the date of said repair. Equipment must be shipped to the factory with transportation prepaid.

Chapter 2 Understanding Hardware for Use

This chapter explains how to configure your Gryphon100 prior to first turn on and use. The following sections will explain how to set up your hardware and to determine if your hardware is functioning.

2.1 Connecting to Hardware

Input and output connections are made to the Gryphon100 rear panel using the BNC connectors or the BD50 connectors.

When working with the Gryphon100's hardware always remember to practice safe electrostatic discharge precautions. Electrostatic discharge or (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials. The term is used to describe momentary unwanted currents that may cause damage to electronic equipment.

2.1.1 Gryphon100 Rear Panel

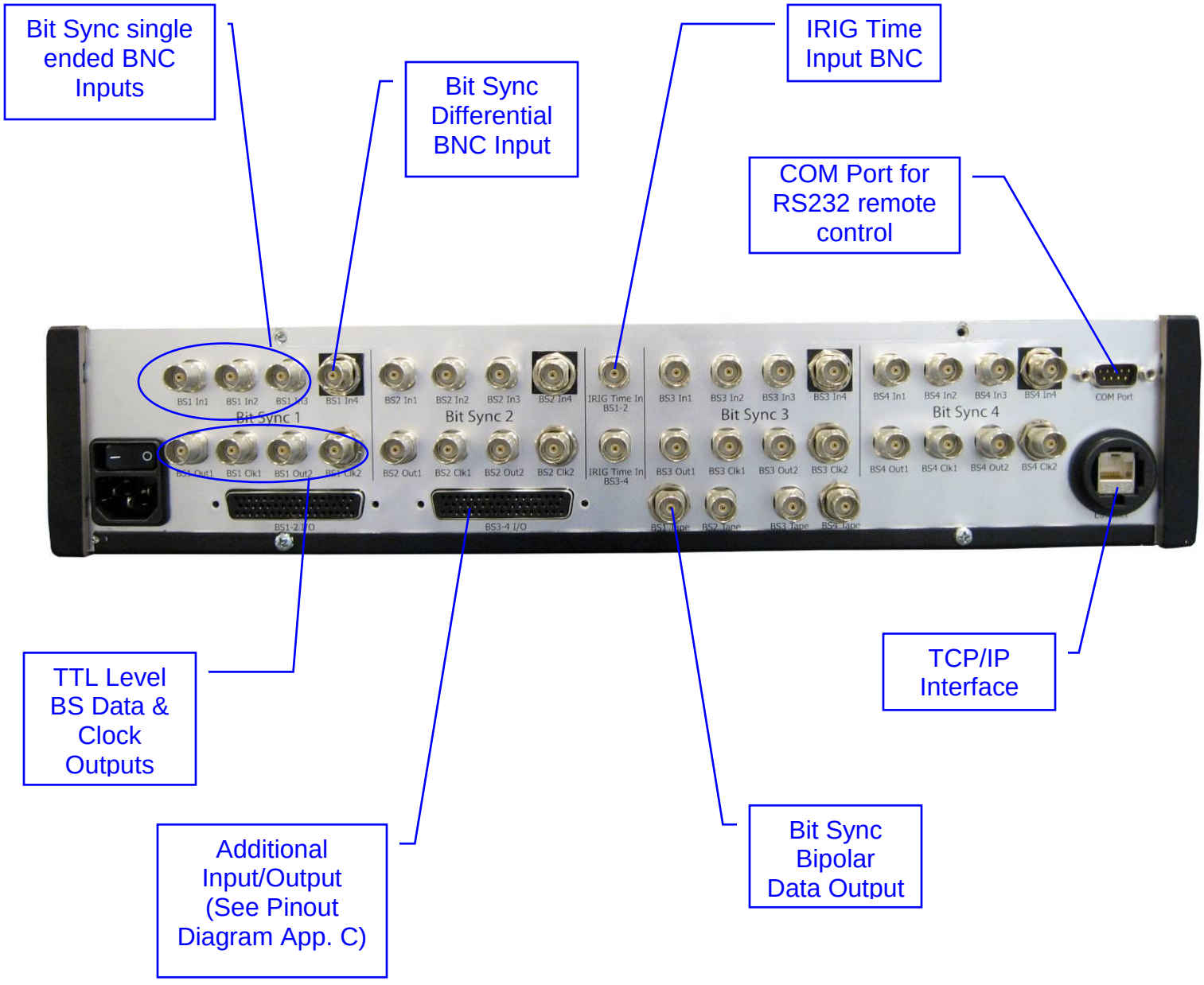


Figure 1 - Gryphon104 Rear Panel Connectors

Connection Location\Label	Connection Function
BS1 In1	Bit Sync1 Input 1
BS1 In2	Bit Sync1 Input 2
BS1 In3	Bit Sync1 Input 3
BS1 In 4	Bit Sync1 Differential Input
BS1 Out1	Bit Sync1 Output 1 (TTL Level)
BS1 CLK1	Bit Sync1 Clock 1 (TTL Level)
BS1 Out2	Bit Sync1 Output 2 (TTL Level)
BS2 In1	Bit Sync2 Input 1
BS2 In2	Bit Sync2 Input 2
BS2 In3	Bit Sync2 Input 3
BS2 In 4	Bit Sync2 Differential Input
BS2 Out1	Bit Sync2 Output 1 (TTL Level)
BS2 CLK1	Bit Sync2 Clock 1 (TTL Level)
BS2 Out2	Bit Sync2 Output 2 (TTL Level)
IRIG Time In BS1-2	Bit Sync1 & 2 Time Input
IRIG Time In BS3-4	Bit Sync3 & 4 Time Input
BS3 In1	Bit Sync3 Input 1
BS3 In2	Bit Sync3 Input 2
BS3 In3	Bit Sync3 Input 3
BS3 In 4	Bit Sync3 Differential Input
BS3 Out1	Bit Sync3 Output 1 (TTL Level)
BS3 CLK1	Bit Sync3 Clock 1 (TTL Level)
BS3 Out2	Bit Sync3 Output 2 (TTL Level)
BS4 In1	Bit Sync4 Input 1
BS4 In2	Bit Sync4 Input 2
BS4 In3	Bit Sync4 Input 3
BS4 In 4	Bit Sync4 Differential Input
BS4 Out1	Bit Sync4 Output 1 (TTL Level)
BS4 CLK1	Bit Sync4 Clock 1 (TTL Level)
BS4 Out2	Bit Sync4 Output 2 (TTL Level)
COM Port	COM Port for RS232 Remote Control
Ethernet	Ethernet Connection
BS1-2 I/O	Bit Sync1 & 2 Additional Inputs/Outputs (See Pinout Diagram App. C)
BS3-4 I/O	Bit Sync3 & 4 Additional Inputs/Outputs (See Pinout Diagram App. C)
BS1 Tape	Bit Sync1 Bi Polar Data Output
BS2 Tape	Bit Sync2 Bi Polar Data Output
BS3 Tape	Bit Sync3 Bi Polar Data Output
BS4 Tape	Bit Sync4 Bi Polar Data Output

2.1.2 Gryphon100 Front Panel

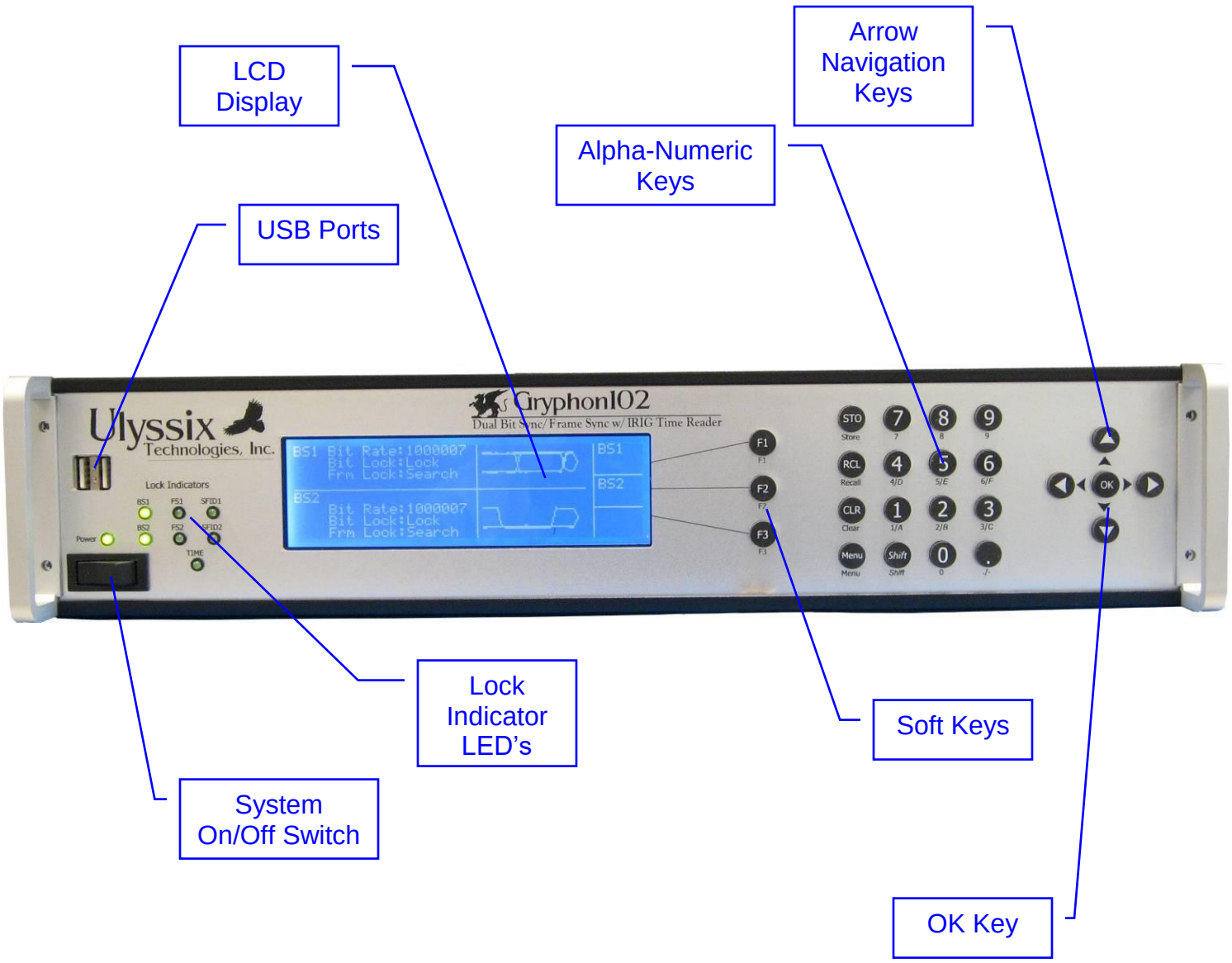


Figure 2 - Gryphon102 Front Panel

Panel Key	Function
F1	Soft Key whose function is displayed on the LCD graphic display in the top right box
F2	Soft Key whose function is displayed on the LCD graphic display in the middle right box
F3	Soft Key whose function is displayed on the LCD graphic display in the bottom right box
STO (Store)	Opens “Save Configuration File” display which allows the current hardware setup to be saved. To customize the Configuration File name press the “OK” key when name is highlighted. Then use the up and down arrows to change between letter/numbers, use the left and right arrows to move your curser. When name completed press OK key to highlight entire name. Then press F1 to store configuration file.
RCL (Recall)	Opens “Load Configuration File” display, where any previously saved hardware setup can be loaded. Any unwanted configuration file can be deleted in this screen by pressing the CLR button.
CLR (Clear)	Clears any highlighted field in the LCD Display
Menu	Opens the Main Menu display
Shift	Allows for the letters on the corresponding number buttons to be used
OK	Opens selected highlighted field in a menu

Table 1 - Front Panel Key Description

2.2 Identifying Hardware Status

2.2.1 LED Indicators

LED Indicators on the front panel of the Gryphon100 provide status for each Bit Sync.

Figure 3 - Gryphon102 LED Indicator Display

LED Labels	LED Function
BS1	Bit Sync1 Lock Indicator
FS1	Frame Sync1 Lock Indicator
SFID1	Sub Frame Sync1 Lock Indicator
BS2	Bit Sync 2 Lock Indicator
FS2	Frame Sync 2 Lock Indicator
SFID2	Sub Frame Sync 2 Lock Indicator
Time1	Time Lock Indicator for channels 1&2
BS3	Bit Sync 3 Lock Indicator
FS3	Frame Sync 3 Lock Indicator
SFID3	Sub Frame Sync 3 Lock Indicator
BS3	Bit Sync 4 Lock Indicator
FS3	Frame Sync 4 Lock Indicator
SFID3	Sub Frame Sync 4 Lock Indicator
Time2	Time Lock Indicator for channels 3&4

Table 2 - LED Function Description

2.2.2 Bit Sync Lock (LOCK)

The Bit Sync Lock LED illuminates green when the Bit Sync's digital phase lock loop has locked onto the incoming PCM signal. If the Lock LED is not illuminated when you expect it

to be locked, please verify the input connections and software settings before contacting the factory for support.

Bit Sync Lock LED may illuminate showing a false Bit Sync Lock. A combination of factors can contribute to momentary false Bit Sync Lock. The Eye Pattern on the ‘Measure Display’ is another indicator of Bit Sync lock.

2.3 Identifying Internal Hardware

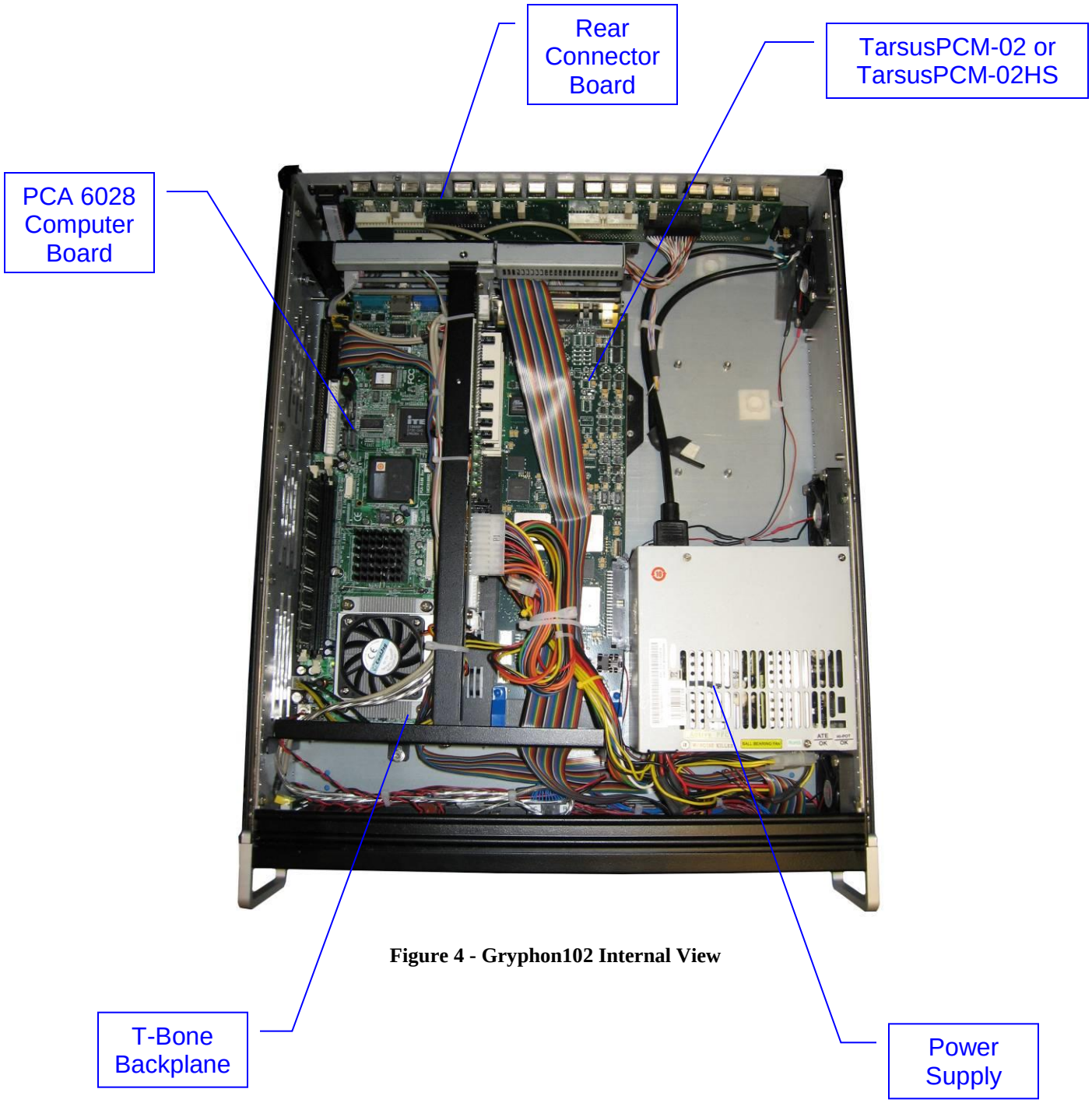


Figure 4 - Gryphon102 Internal View

Chapter 3 Basic Operations

3.1 Startup

3.1.1 Power Switches

The switch on the back panel of the Gryphon100 chassis located above the power cord has an "–"(on) position and "o" (off) position. To turn on the power switch make sure the "-"(on) side is depressed.

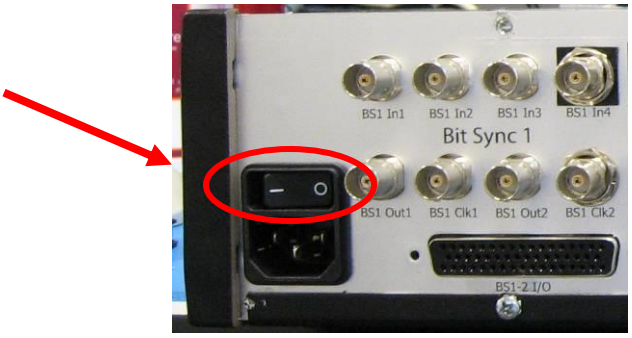


Figure 5 - Gryphon100 Rear Panel Power Switch

Once the rear switch is placed in the on position the front momentary rocker switch can be held down until the LEDs on the front of the chassis start to cycle then the switch can be released. Make sure you hold the rocker switch all the way down until the LEDs cycle.

Figure 6 - Gryphon100 Front Panel Rocker Power Switch

If the LED's do not start to cycle when the rocker switch is held down make sure the power cord is plugged in all the way and the rear power switch is in the "-"(on) position.

3.1.2 Startup Display

During the sixty second startup the Lock Indicator LEDs on the front panel of the Gryphon100 will perform a cycling pattern. The LCD display will stay in a startup screen while the embedded operating system configures the hardware components.

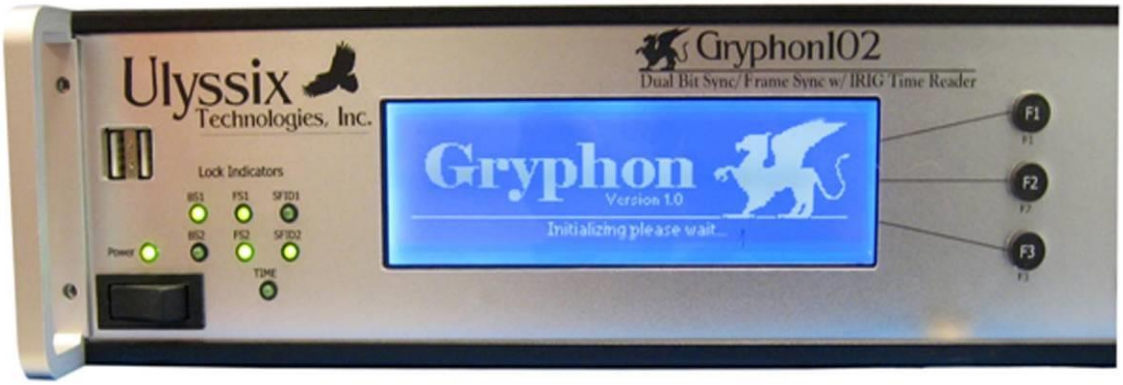


Figure 7 - Gryphon 102 Startup LCD Display

3.2 Shutdown

To shut the Gryphon100 down, hold the rocker switch on the front panel down until the LEDs start to cycle. Then the Gryphon100 shutdown process takes roughly thirty seconds. The shutdown display is displayed while the embedded operating system configures the hardware for shutdown.

Figure 8 - Gryphon102 Shutdown LCD Display

Using the rear Power Switch to shutdown the system may lead to a loss of data. A proper shutdown is necessary for data changed during a session (eg. Format files saved, software upgrade) to be written to the operating image that will resume on startup.

Chapter 4 Introducing the Main Screen

The Gryphon100 provides a simple to user interface allowing the user to control and analyze data. The main screen of the Gryphon100 gives the user a full view of all the display choices. All configuration, setup and data displays can be launched from the main screen.

Figure 9 - Main Menu Screen Display

1. **Measure –** This menu selection is used to bring up the measure screen displaying the incoming data streams.
2. **BitSync –** This menu selection is used to bring up the Bit Sync configuration menu.
3. **Frame Sync –** This menu selection is used to bring up the Frame Sync configuration menu.
4. **IRIG Time –** This menu selection is used to bring up the IRIG Time configuration menu.
5. **Outputs –** This menu selection is used to bring up either Bit Sync Output setups
6. **Archive –** This menu selection is used to bring up the Archive menu**.**
7. **FPGA Upload –** This menu selection is used to upload new firmware to the internal TarsusHS-02 board
8. **SW Upgrade –** This menu is used to upgrade the Gryphon software on the unit
9. **Scope –** This menu selection is used to display the built in scope of the incoming data stream
10. **Remote –** This menu selection allows access to the setup of both TCP/IP and RS232 remote programming

Figure 10 Extended Menu Screen

1. **DQ Encapsulator –** Optional feature which allows quality information added to bit stream for help in Best Source Selection of encrypted channels.
2. **Viterbi Setup –** Optional feature which opens setup of Viterbi Decoder.
3. **Debug –** This menu selection is used to debug a hardware problem with factory assistance

Chapter 5 Configuring the Gryphon100

The menu tree of the Gryphon100 is designed for quick sequential setup of all pieces of the hardware. For example, the Frame Sync setup can be accessed from the Bit Sync setup screen.

5.1 Configuring the Bit Sync

To configure the Bit Sync, follow the procedure below.

There are two ways to access the Gryphon100 Bit Sync Setup screen. From the Startup Measure screen:

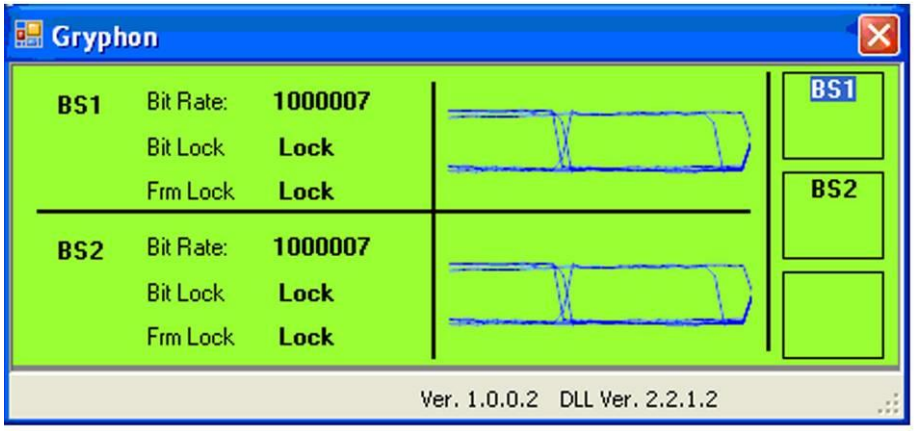


Figure 11 - Bit Sync Measures Screen Display

Depress the **F1** key for the "Bit Sync 1 Setup" or press **F2** key to select the "Bit Sync 2 Setup" menu

The Other option to access "Bit Sync Setup" is through the Main menu (see Figure 11). Select the number **2** key or use the Arrow keys and then select **OK**.

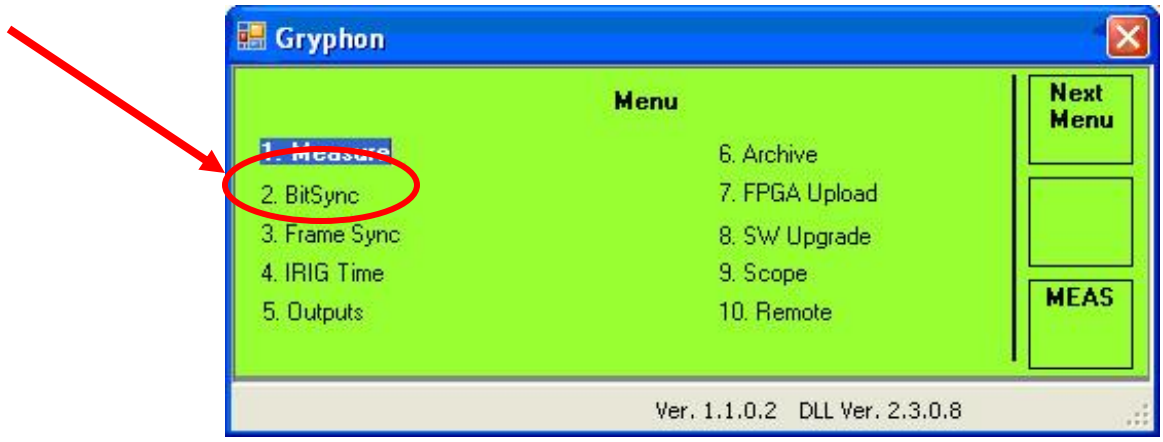


Figure 12 - Main Menu Screen Display

Use this Bit Sync Setup window (Figure 12) as a reference while following the step by step setup.

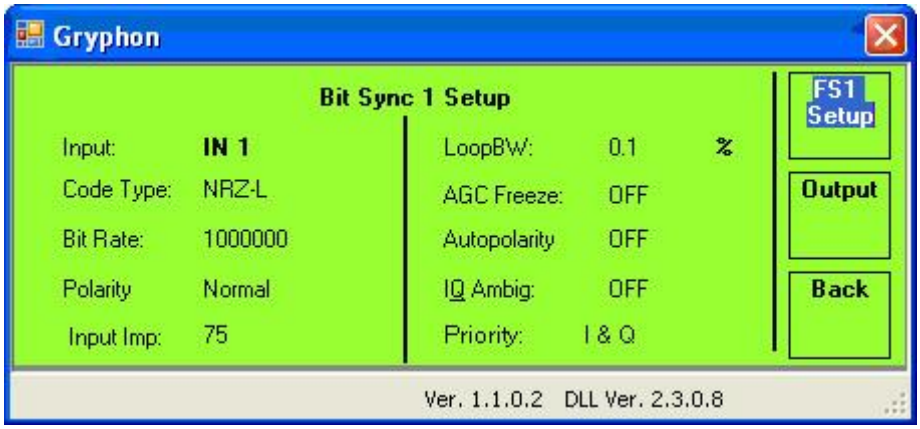


Figure 13 - Bit Sync Setup Screen Display

1. Select an input connection; either **IN 1, IN 2, IN 3, IN 4 Diff**. Each input references a rear BNC connector. When an input is selected, the bit sync will be receiving data via the corresponding rear panel connection. If **IN 4 Diff** is selected, the hardware is expecting a differential signal via the 4th input BNC.

The Hardware uses a switch to choose the inputs; only one is active at a time.

2. Select the appropriate code type for the incoming PCM stream.

3. Enter the bit rate of the incoming PCM stream. The rate must be entered in bits per second (**bps**).

4. Enter a Loop BW setting in the range of 0.01 to 3.00 percent. Using a smaller Loop BW setting will achieve better bit error performance out of the Bit Sync, however if the input PCM data rate is slightly low or high a lock may not occur.

5. If the polarity is unknown, select Auto Polarity. The software will determine the polarity based on frame lock status.

6. Next, select the "Output Setup" Screen by pressing the **F2** Key.

Figure 14 - Bit Sync Setup Screen Display

7. Now select the PCM code type for the first output of the Bit Sync. The output code types are; non-return to zero level (**NRZ_L)**, non-return to zero mark (**NRZ_M)**, non-return to zero space (**NRZ_S)**, bi-phase level (**BIΦ_L)**, bi-phase mark (**BIΦ_M)**, bi-phase space (**BIΦ_S)**, return to zero (**RZ)**, randomized non-return to zero **RNRZ_11** and **RNRZ_15** and are completely independent from the input type.

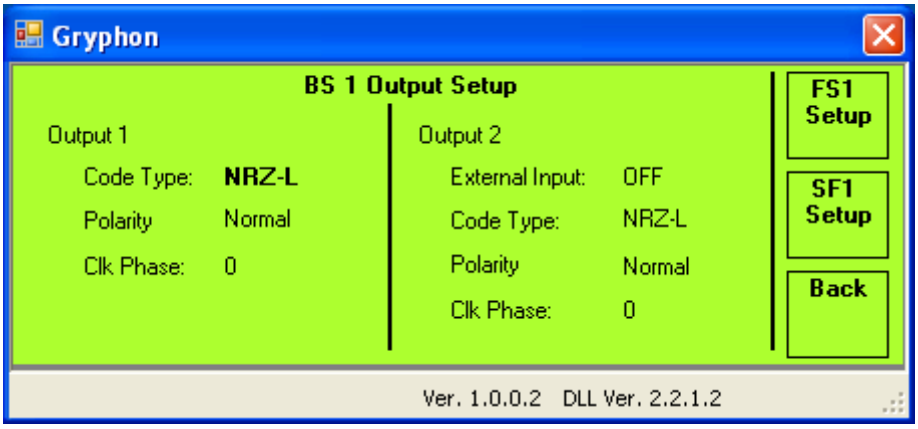


Figure 15 - Bit Sync Out Setup Screen Display

8. Select either **Normal** or **Inverted** polarity for the output PCM data stream.

9. Select a clock phase of **0**, **90**, **180** or **270** degrees. This setting will change the relationship of the data with respect to the PCM clock rising edge. The proper setting here will depend entirely on the type of external equipment being attached.

10. To setup a second Bit Sync output for the same input signal repeat steps 7-9 for the "Output 2" section of the display.

11. Select **Use External Input** if the second output is to be used as a standalone code converter.

Clicking OK does not save the changes to the computer hard drive or send them to the hardware; it simple stores these changes to the in-memory database. Saving and downloading must be done using the **STO** and **RCL** buttons

5.2 Using I & Q Ambiguity

With the advancement of quadrature phase modulation techniques has come a need to compensate for an I & Q ambiguity of the two resulting streams. In the Gryphon100 we have incorporated a feature to determine stream identity (I or Q) using Frame Lock.

If a signal is transmitted using a modulation technique vulnerable to I & Q swapping, there are four possible states a channel may be in at any moment.

Channel
I
-I (inverted)
Q
-Q (inverted)

In the Gryphon software, the user selects which states are possible for a given channel. Enabling Auto Polarity tells a channel to flip polarity when not in frame lock. Enabling IQ Ambiguity tells the channels to swap inputs (BS1 receives BS2's input and vice versa). Both features are independent, the user can enable Auto Polarity, I & Q Ambiguity, or both.

Setting the IQ Priority tells the unit how to cycle through states. A priority of I & Q instructs the unit to attempt swapping inputs prior to polarity; vice versa is true for a priority of Polarity. If none or only one ambiguity is enabled (I & Q or Auto Polarity) then priority is not applicable.

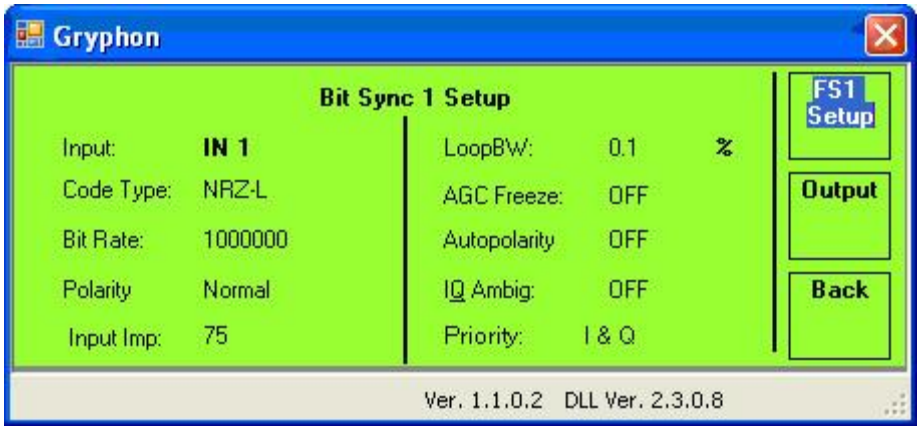
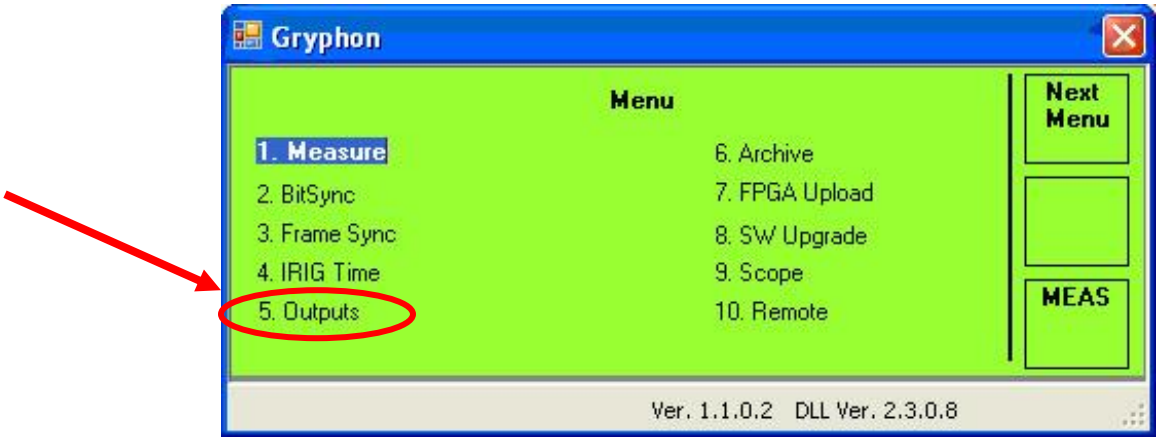


Figure 16 Bit Sync Setup Screen

5.3 Configuring Bit Sync Outputs

The Gryphon is equipped with two independent Data and Clock outputs and 1 Tape output per Bit Sync. The Data and Clock outputs are TTL and the Tape output is bipolar.

To access the Output Setup, Select **F2** or **Output** from the Bit Sync Setup form or from the Menu screen select **5. Outputs**.



Both Data and Clock output sets are independent for each bit sync. They can have different code types as well as polarities and clock phases. The second output can be used as a code converter (independent from Bit Sync) by enabling External Input (refer to Appendix C for pinout).

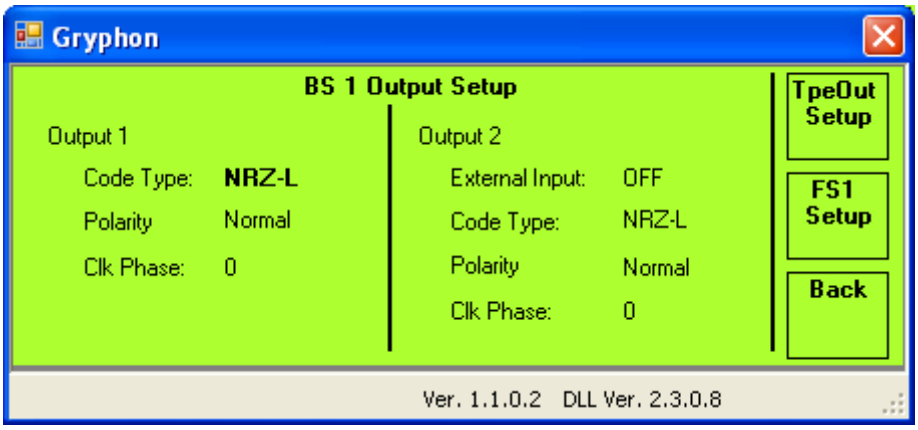


Figure 17 Bit Sync Outputs Setup Screen

The Tape output for each bit sync is a configurable analog data output. The output level and offset are adjustable. The Tape output uses the same code type and polarity as one of the first outputs; this is selectable.

Figure 18 Tape Output Setup Screen

To access the Tape Output setup, select F1 or TpeOut from the Bit Sync Output Setup screen. Both Bit Sync Tape outputs are configured from this screen. The only fields that are changeable are:

- SRC – source that the Tape out mimics (code type and polarity): Out1 or Out2.
- Level – Volts Peak to Peak for the output signal.
- Offset – DC voltage offset to the signal. 0 VDC offset will be a bipolar signal centered at 0V.

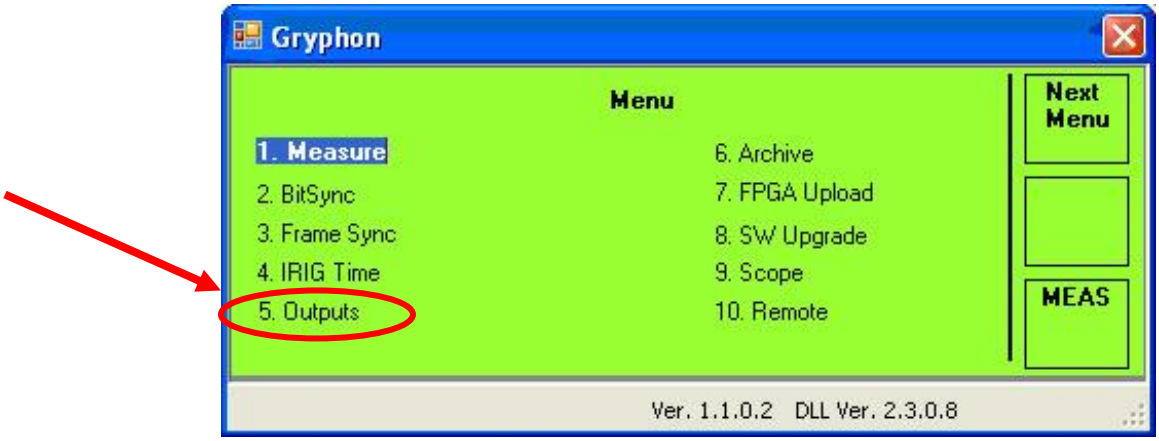
5.4 Using I & Q Interleaving

The Gryphon100 can interleave the data from Bit Sync 1 and Bit Sync 2 into a single stream. This interleaving is a bit for bit combining of the data. The Output 1 of Bit Sync 1 will be the concatenated stream.

To set up the hardware, first feed the I-channel into Bit Sync 1 and the Q-channel into Bit Sync 2. If the unit is a Gryphon104, the I and Q can also be fed into Bit Sync 3 and Bit Sync 4, respectively.

To set up the unit for I & Q interleaving, first navigate to the Bit Sync Outputs Setup of Bit Sync 1 (if the unit has four bit syncs, then Bit Sync 3 will also allow the I & Q Interleave setup).

To access the Output Setup, Select **F2** or **Output** from the Bit Sync Setup form or from the Menu screen select **5. Outputs**. Then Select Bit Sync1 Output.



On the Bit Sync Outputs Setup form there are two selections for **Interleave** and **IQ Order**. These are the controls for the I & Q Interleaving.

To enable interleaving, use the **Down Arrow** to navigate to the **Interleave** field. Then use the right or left arrow to change the selection and enable / disable the I & Q Interleaving.

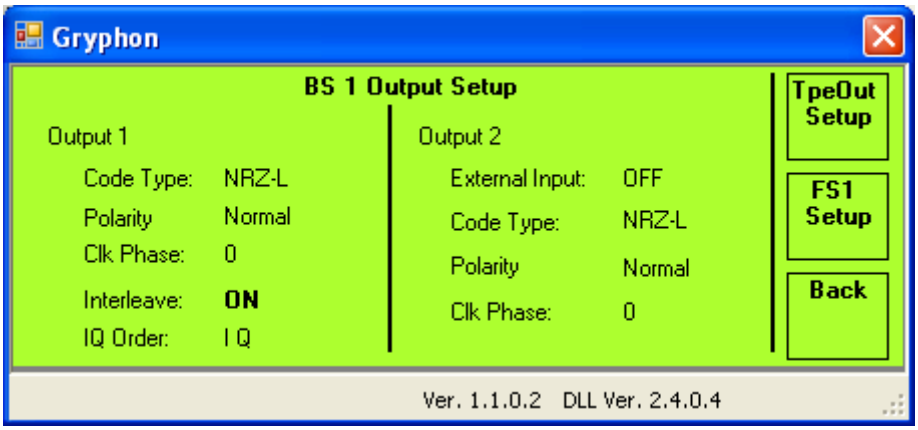


Figure 19 I & Q Interleaving Setup

If the **Interleave** field displays ON, the unit will now be combining the Bit Sync 1 and 2 streams.

To change the order in which the streams are combined, navigate to the **IQ Order:** field and use the right or left arrow to change between **'I Q'** and **'Q I'**. This field is assuming **I = Bit Sync1** data and **Q=Bit Sync2** data.

When Interleaving is enabled, an 'I' will appear on the main status screen as an indicator.

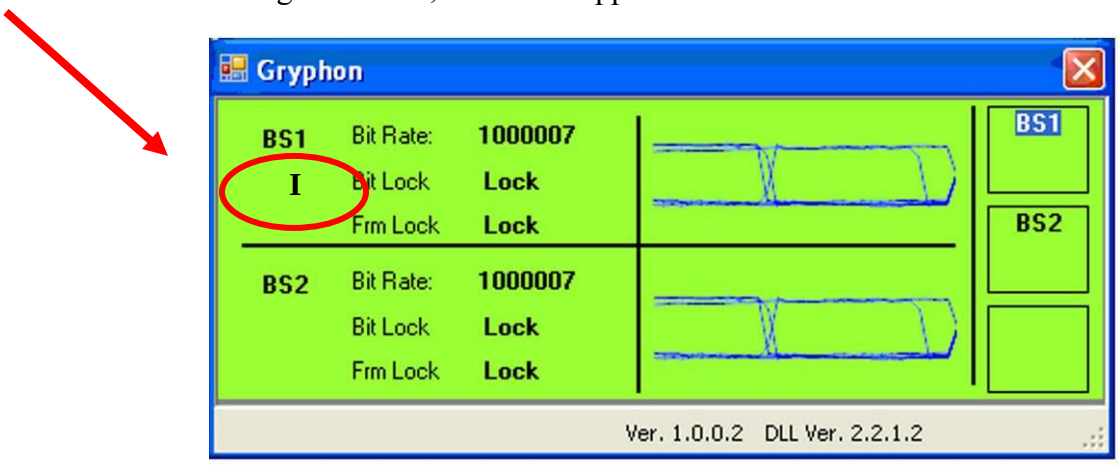


Figure 20 Interleave Indication

5.5 Configuring the Frame Sync

To configure the Frame Sync, follow the step by step procedure below.

At the Gryphon100 Main menu screen select a Frame Sync by either pressing the number **3** key or by using the Arrows and selecting **OK**.

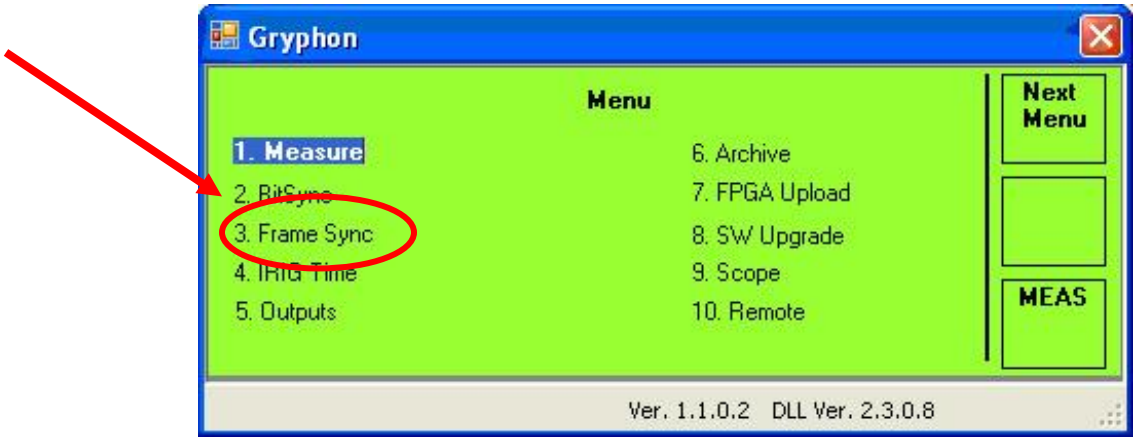


Figure 21 - Main Menu Screen Display

Use this Frame Sync Setup window (Figure 16) as a reference while following the step by step setup.

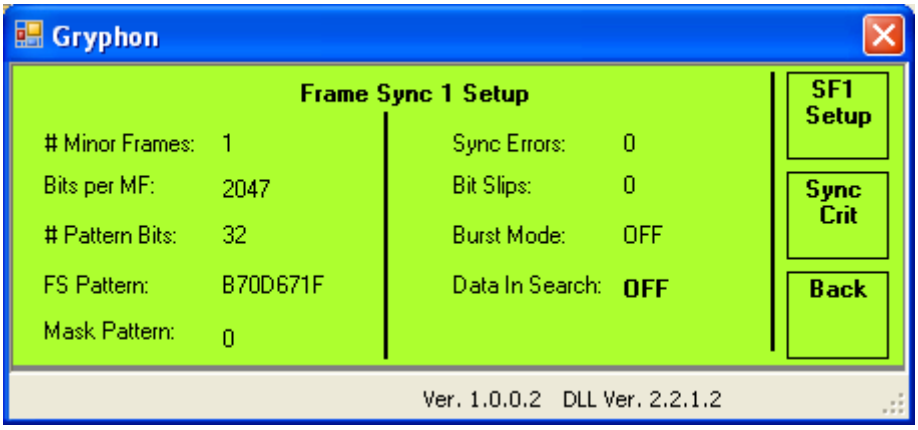


Figure 22 - Frame Sync Setup Screen Display

1. Enter a number from **1** to **1024** for the number of minor frames in a major frame.

2. Enter the total number of bits in a minor frame including the bits in the Frame Sync Pattern.

3. Enter the number of Frame Sync Pattern bits from **16** to **33** bits.

4. Enter or select the appropriate sync pattern for the incoming PCM stream.

5. Select the **Use Mask** to setup a mask value that will cause the Ulyssix frame sync circuitry to ignore certain bits of the sync word. If using mask, go to step 6, otherwise skip to step 7.

6. Enter a mask value using the following logic rules: logic high or '1' in any bit position will cause the Frame Sync circuitry to ignore that bit. For example:

   Frame Sync Pattern length: 32 bits
   Sync pattern : FE6B2840 (in Hexadecimal)
   Mask value : 0000F000 (in Hexadecimal)

   This example will cause the Frame Sync circuit to ignore bits 12 through 15 during sync detection. Any value in the PCM stream where the **"2"** in the FE6B2840 pattern is located would cause a valid frame lock.

7. Enter the number of Frame Sync Pattern errors the frame sync circuitry are allow in the incoming PCM stream before declaring the frame is not in lock. NOTE: A sync error is defined as any bit within the frame sync pattern data that is not masked and does not match the entered frame sync pattern. A non-allowed sync error will cause a transition in the sync criteria explained in steps 9-12 below.

8. Enter the number of bit slips the frame sync circuitry should allow in the incoming PCM stream before declaring the frame is not in lock. A non-allowed bit slip will cause a transition in the sync criteria explained in steps 9-12 below.

9. Use the Data In Search Mode selection if the user desires data regardless of the Frame Lock status.

10. Use the Burst Mode selection if the expecting data is a limited number of minor frames in a burst followed by filler data.

11. Setup the sync match criteria press the **F2** key to bring up the "Sync Criteria" screen.

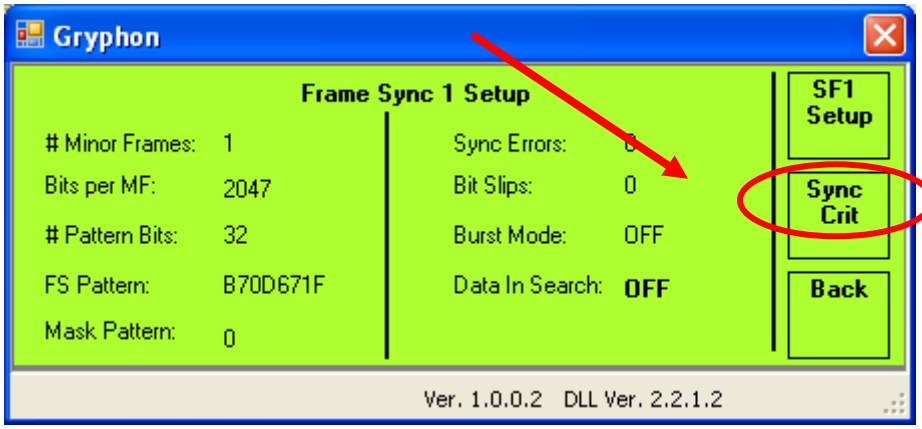


Figure 23 - Frame Sync Setup Screen Display

Use this Frame Sync Criteria Setup window as a reference while following the step by step setup.

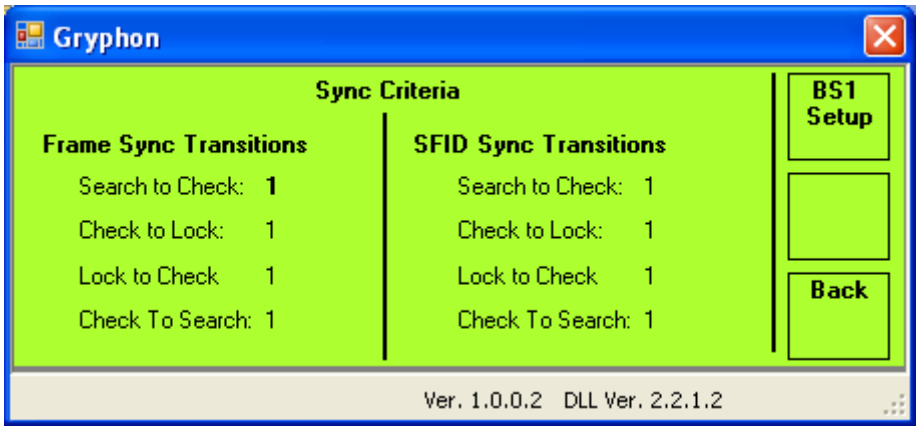


Figure 24 - Frame Sync Criteria Setup Screen Display

12. Set up the Sync Criteria by setting the number "Search to Check" transitions the hardware requires before the frame sync status promotes from ***Search*** to ***Check***.

13. Set the number “Check to Lock” transitions the hardware requires before the frame sync status promotes from ***Check*** to ***Lock***

14. Setup the sync miss criteria by setting the number “Lock to Check” transitions the hardware requires before the frame sync status demotes from ***Lock*** to ***Check***.

15. Set the number “Check to Search” transitions the hardware requires before the frame sync status demotes from ***Check*** to ***Search***.

Clicking OK does not save the changes to the computer hard drive or send them to the hardware; it simple stores these changes to the in-memory database. Saving and downloading must be done using the **STO** and **RCL** buttons.

5.6 Configuring the Sub Frame Sync

To configure the Sub Frame Sync, follow the step by step procedure below.

At the Gryphon100 Main menu screen select a “Frame Sync” by either pressing the number **3** key or by using the Arrows and selecting **OK**.

Figure 25 - Main Menu Screen Display

Use the Frame Sync Setup window to access the Sub Frame Sync menu by pressing the **F1** Key.

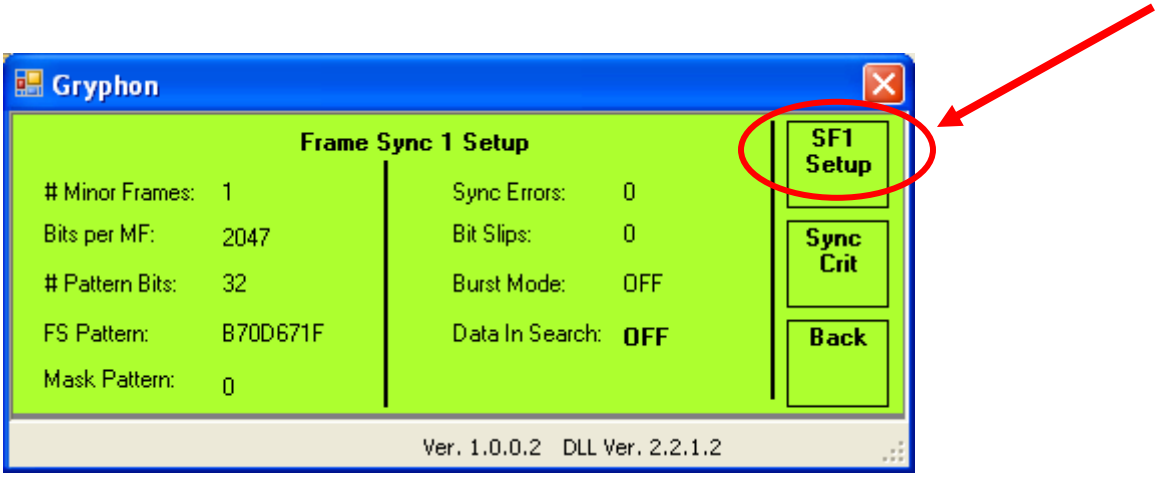


Figure 26 - Frame Sync Setup Screen Display

Use this "Sub Frame Sync Setup" window (Figure 21) as a reference while following the step by step setup.

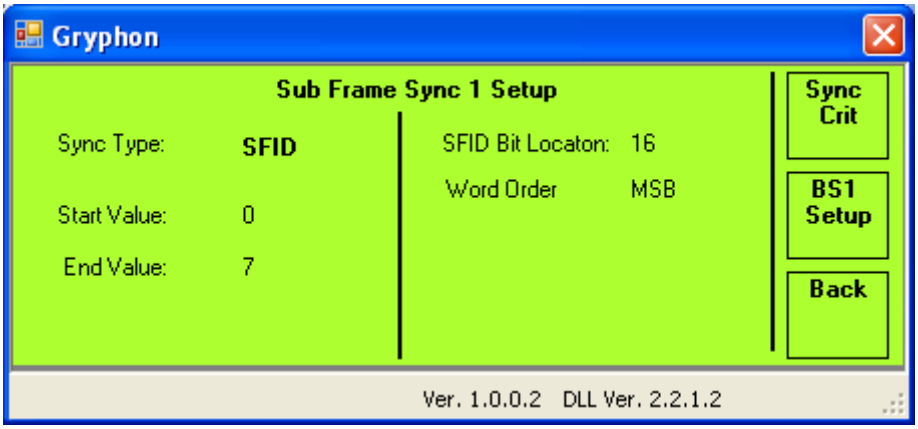


Figure 27 - Sub Frame Sync Setup Screen Display

1. Select the Sub Frame synchronization method. Select either Sub Frame ID counter (**SFID**), Frame Code Complement (**FCC**) or No minor frame sync (**None**). If **SFID** is selected, go to step 2, otherwise skip ahead to step 6.

2. Setup the SFID by entering the number of bits from the beginning of the frame to the least significant bit (LSB) of the SFID word, not including the Frame Sync Pattern. For example, if the SFID word was located at word location 1 and the data was transmitted most significant bit first (MSB), the number of bits would simply be the size of the SFID word.

3. Select either MSB or LSB to set the bit order of the SFID transmission in the PCM stream.

4. Enter a starting and ending value for the SFID. Typically, this would start at zero and end at the number of minor frames minus one.

5. Press the **F1** Key to access the Sub Frame Sync Criteria Screen.

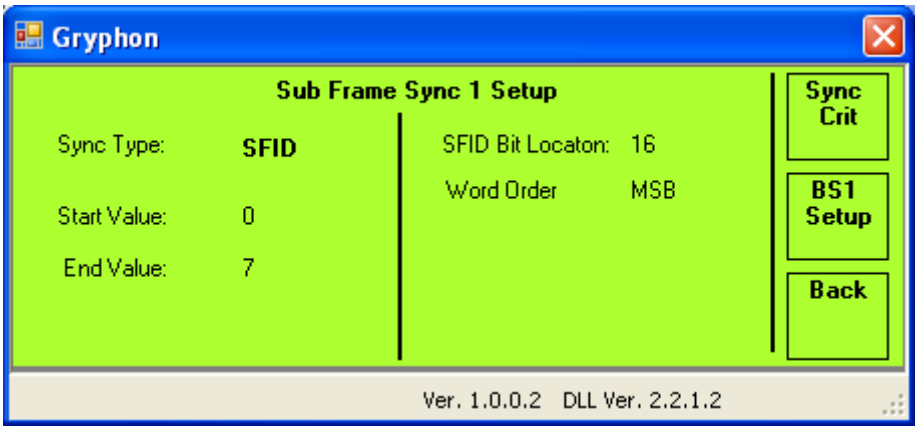


Figure 28 - Sub Frame Setup Screen display

Use this Sync Criteria window as a reference while following the step by step setup.

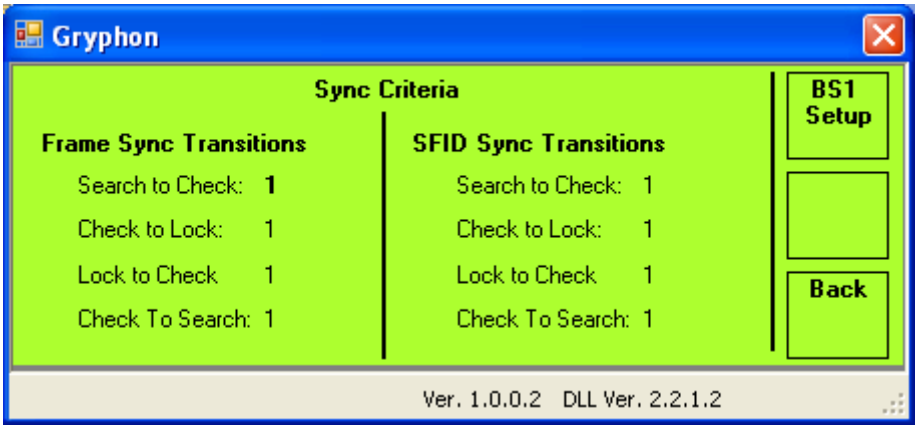


Figure 29 - Frame Sync Criteria Screen Display

6. Setup the sub frame sync match criteria by setting the number "Search to Check" transitions the hardware requires before promoting the frame sync status from ***Search*** to ***Check***.

7. Set the number "Check to Lock" transitions the hardware requires before promoting the frame sync status from ***Check*** to ***Lock***.

8. Setup the sub frame sync miss criteria by setting the number "Lock to Check" transitions the hardware requires before demoting the frame sync status from ***Lock*** to ***Check.***

9. Set the number "Check to Search" transitions the hardware requires before demoting the frame sync status from ***Check*** to ***Search***.

Clicking OK does not save the changes to the computer flash drive; it simply stores these changes to the in-memory database. Saving and downloading must be done using the **STO** and **RCL** buttons.

5.7 Configuring Time

The Gryphon100 system time stamps the PCM data. There are two methods for acquiring time: IRIG time or Computer time. IRIG Time requires an external IRIG time signal. Computer time uses the clock on the internal computer.

The Gryphon100 system has two Bit Syncs per IRIG Time Code reader. Bit Sync 1 and Bit Sync 2 share an IRIG Time Code reader. Bit Sync 3 and Bit Sync 4 share a different IRIG Time code reader.

- **Time Code Reader** – The time code reader is separate hardware circuitry in the Gryphon100 that will read IRIG-A, IRIG-B, IRIG-G, and NASA-36 from an independent input.

1. At the Gryphon100 Main screen, select the **IRIG Time** window by either pressing the number **4** Key or using the Arrows and selecting **OK.**

Figure 30 - Main Menu Screen Display

Use this IRIG Time window (Figure 30) as a reference while following the step by step setup.

Figure 31 - IRIG Time Setup Screen Display

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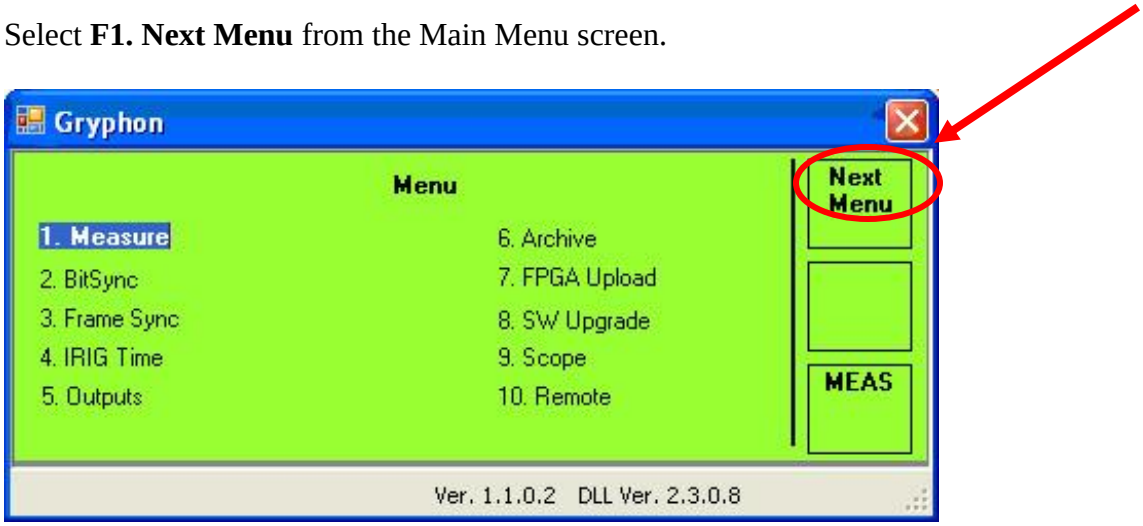
2. Next, for the **IRIGReader,** select from **IRIG-A**, **IRIG-B**, **IRIG-G or NASA-36** by using the arrow left or arrow right keys.

3. Select to turn on or off the Flywheel function. This function allows for the hardware to interpolate time if there is a loss of the signal.

5.8 Configuring Viterbi (option)

The Gryphon100 unit has an optional Viterbi Decoder built into each bit sync. Using a 7-bit Soft Bit Decision, this algorithm allows for the decoding of a convolutionally encoded signal, resulting in a 3-5 dB improvement in noise tolerance. To use this licensed feature:

1. Select **F1. Next Menu** from the Main Menu screen.



2. Next select **Viterbi Setup**, if the feature is not licensed a screen will display indicating such. Contact the factory to purchase this option (301-846-4800).

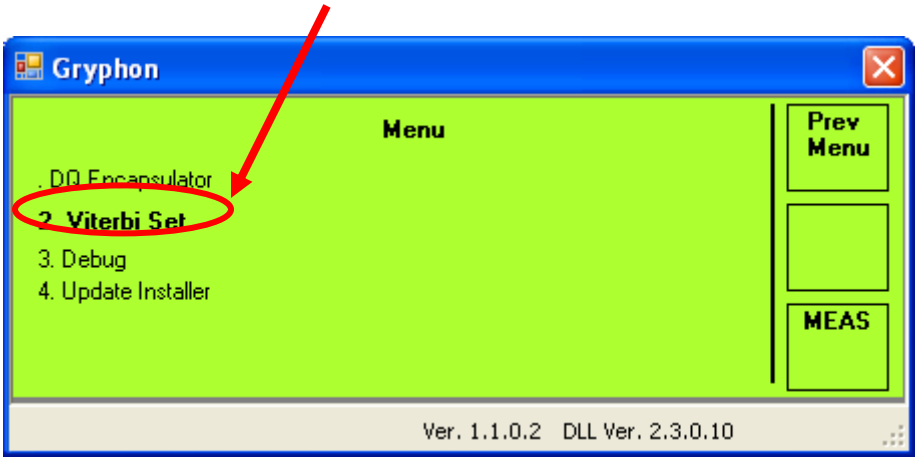


Figure 32 - Extended Menu Screen

3. On the Viterbi Setup Screen has options to both enable the Viterbi Decoder and select the order and polarity of G1 and G2 for the first two bit syncs.

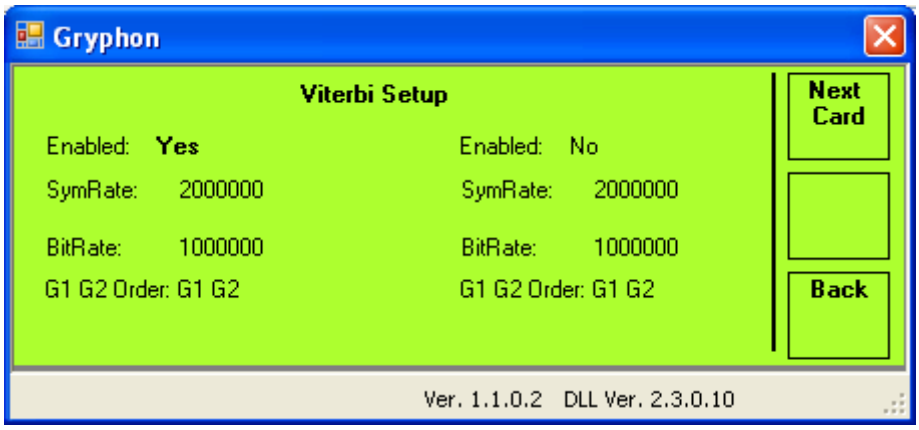


Figure 33 - Viterbi Setup Screen

On the Viterbi Setup Screen, there are four fields to program the Viterbi Decoder.

1. The **Enable** field turns the Viterbi Decoder on and off.

2. The **SymRate**: field sets the incoming symbol rate. Since the Ulyssix decoder currently only handles a rate of 1/2; the SymRate is always two times the BitRate (or data rate). This is automatically updated.

3. The **BitRate** is defined as the output data rate. Setting this field automatically changes the SymRate field to twice the data rate entered.

4. **G1 G2 Order** refers to the order and polarity of the G1 G2 bits of the incoming data stream. There are 8 possible states for the G1 G2 order and polarity. Use the Arrow Keys to cycle through and select the appropriate one.

A negative (-) sign in front of a G*x* indicates its polarity should be inverted.

Ulyssix utilizes a seven soft bit Viterbi algorithm, giving our decoder better noise rejection than other decoders.

5.9 Configuring CRC (option)

The Gryphon100 unit has an optional **Cyclic Redundancy Check (CRC)** algorithm incorporated into each channel. The CRC option is A 16-bit CCITT algorithm used to detect data bit errors within a minor frame boundary. The CRC calculation is performed on all bits (excluding the CRC itself) within the minor frame. The hardware processes the CRC calculation and determines the validity of each minor frame in real time. Below are descriptions of various variables, calculations, and feedback of the CRC algorithm.

CRC Setup

Enable:

The Enable field turns On or Off the CRC of the selected channel. Each channel is independent, so one can be enabled while the other is disabled without trouble. However, if the best source selection is set to CRC, both CRC channels must be enabled.

Output Buffer:

The minor frame validity is determined at the end of each minor frame (location of the CRC words). With the buffer off, the CRC-valid output signal will transition and hold AFTER the frame in question. The CRC-valid signal will thus be offset by one frame. With the buffer on, the CRC data output is delayed (until the minor frame validity is determined) as to synchronize the CRC-valid signal with the appropriate minor frame.

Samp Int:

The sample interval is the number of minor frames that will be used in the Frame Error Rate (FER) calculation. Each time the selected number of frames passes, the FER calculation will be repeated and displayed on the screen. To prevent overwriting to the display, a Samp Int resulting in an update faster than 0.5 seconds is not allowed.

Best Src:

The Best Source Selection of 2 channels can be performed using either Frame Lock Status (FS) or CRC validation (CRC). If FS is selected, the channel with a valid Frame Lock will be output via BS1 OUT and BS1 CLK. CRC does not have to be enabled for FS best source selection to function. If CRC is selected as the Best Src: the stream with no error in CRC will be output via BS1 OUT and BS1 CLK. The CRC of both channels must be enabled if Best Src: is set to CRC for the selection to function correctly.

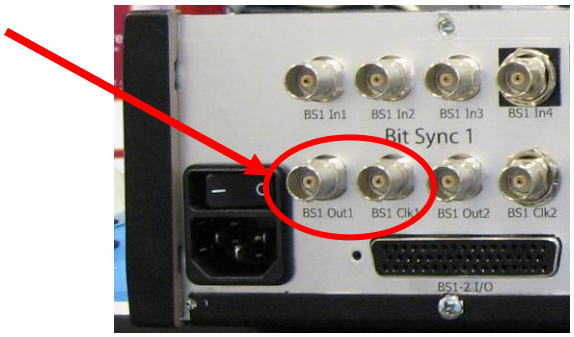


Figure 34 - Best Source Output

CRC Status

Errors:

The Errors field displays the current error count of the specified CRC channel. Each error represents a minor frame which failed CRC validation. The error counter has a maximum value of 16777216 at which point the channel must be reset to begin the count again.

Minor Frames:

The Minor Frames field displays the count of minor frames that have been evaluated by the CRC algorithm. This field, as well, has a maximum value of 16777216 at which point the channel must be reset for the count to continue.

Ratio:

The Ratio field displays the calculation of Errors per Minor Frame. This calculation uses the overall Error count divided by the overall Minor Frame count.

FER:

The Frame Error Rate (FER) field displays the calculation of the rate at which minor frame errors are occurring. This calculation uses the Sample Interval to determine when to perform the calculation. For example, if the Samp Int is set to 2^10, the FER calculation will be performed every 1024 minor frames. Since this calculation does not use overall errors or minor frames, it provides a more instantaneous calculation of the errors being received.

Feed Back

Frame Valid Signal:

This output of the rear DB50 indicates whether a minor frame has passed the CRC test. While the signal is high (TTL level) the minor frames are valid. When the signal is low, the data is not valid according to the CRC algorithm.

CRC Minor Frame Valid Signal Locations *(See App. C for complete pin out)*-

Gryphon102

CRC1 = pin 16

CRC2 = pin 35

Gryphon104

CRC1 = pin 16 (of first DB50)

CRC2 = pin 40 (of first DB50)
CRC3 = pin 16 (of second DB50)
CRC4 = pin 40 (of second DB50)

Figure 35 - DB50 Location

5.9.1 Setup of CRC

1. From the **Main Menu** screen, select **F1 Next Menu** to open the extended menu screen.

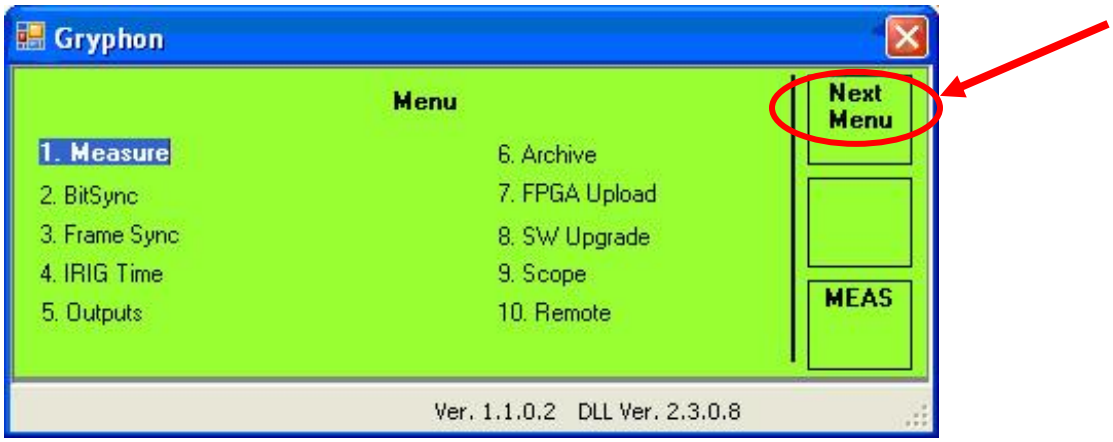


Figure 36 - Main Menu Screen

2. From the extended Menu screen select **Cyclic Redundancy Check** to access the setup of the CRC.

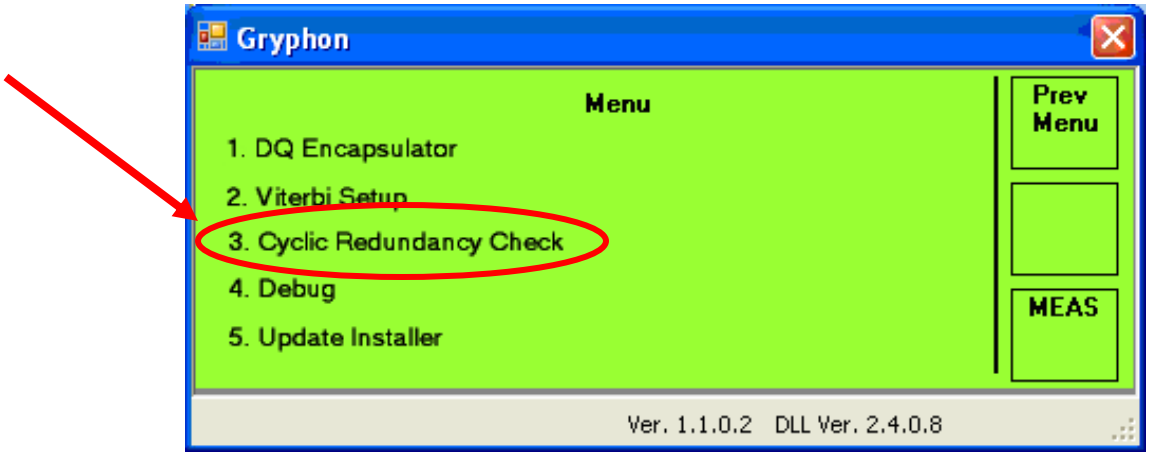


Figure 37 - Extended Menu Screen

3. In the **CRC Setup screen**, the user has the ability to configure both channels of CRC independently. To enable a CRC channel, use the up and down keys to navigate to the **Enable** field. Then use the right and left arrow keys to enable or disable the CRC.

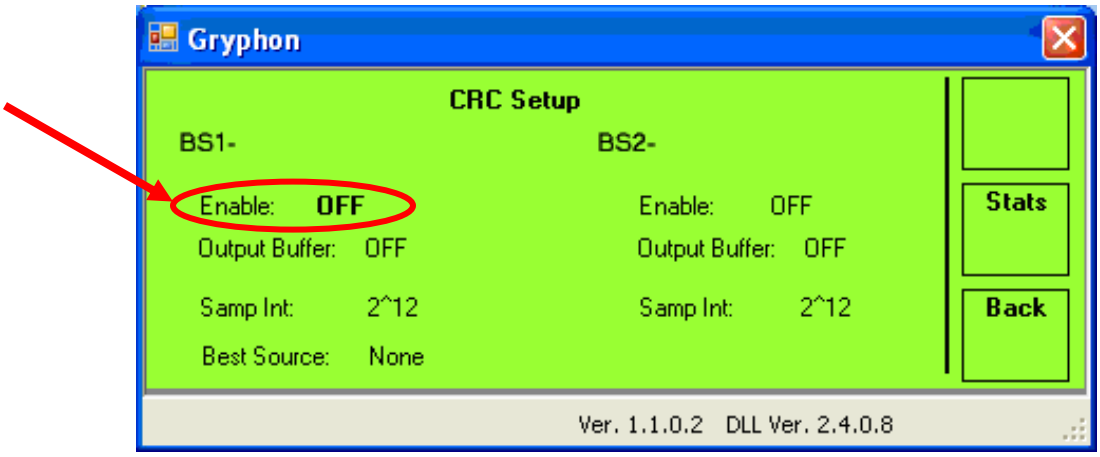


Figure 38 - CRC Enable

4. To enable a channel's **Output Buffer**, navigate to the Output Buffer field and use the right and left arrow keys to enable or disable the feature.

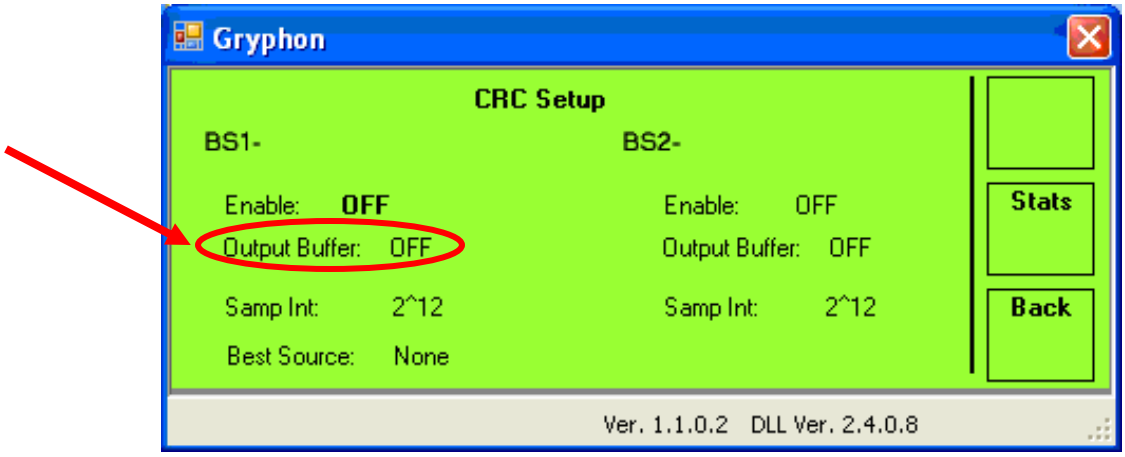


Figure 39 - CRC Output Buffer Enable

5. To change the Sample Interval, navigate to the **Samp Int** field and use the right and left arrow keys to move between the selections.

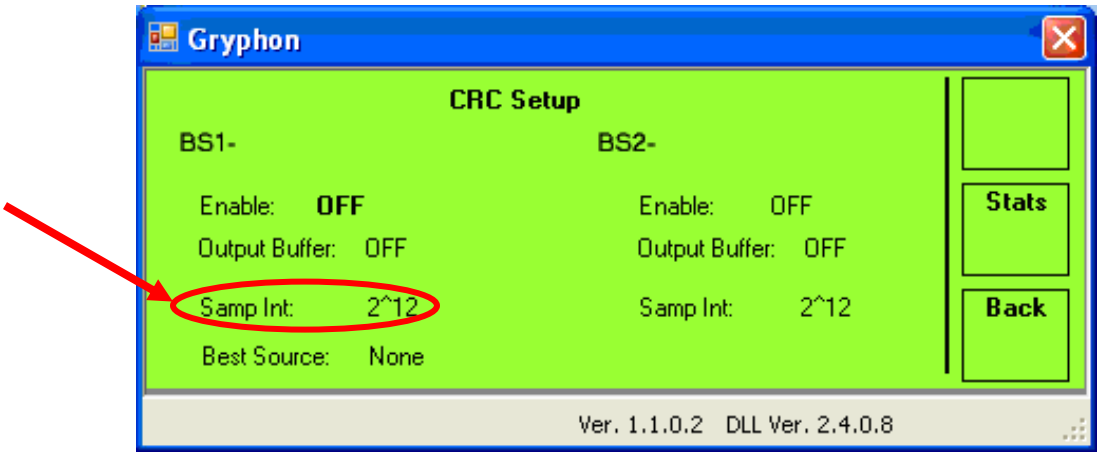


Figure 40 - CRC Sample Interval Selection

6. To Enable the **Best Source Selection** of the two channels, navigate to the **Best Src:** field and use the right and left arrow keys to select the different options. If **Best Src:** is set to **CRC** and either of the CRC channels are not enabled, a warning message will appear at the bottom of the screen to remind the user that both CRC channels must be enabled for the Best Source Selection based on CRC errors to function properly.

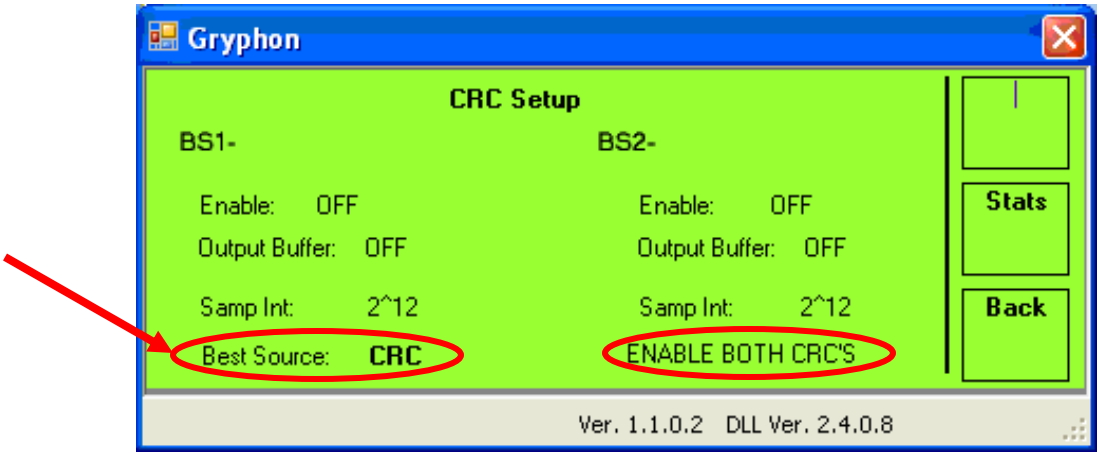


Figure 41 - Best Source Selector Enable

5.9.2 Reading CRC Status

1. From the CRC Setup form, Select **F2 Stats** to open the CRC Status screen for both channels.

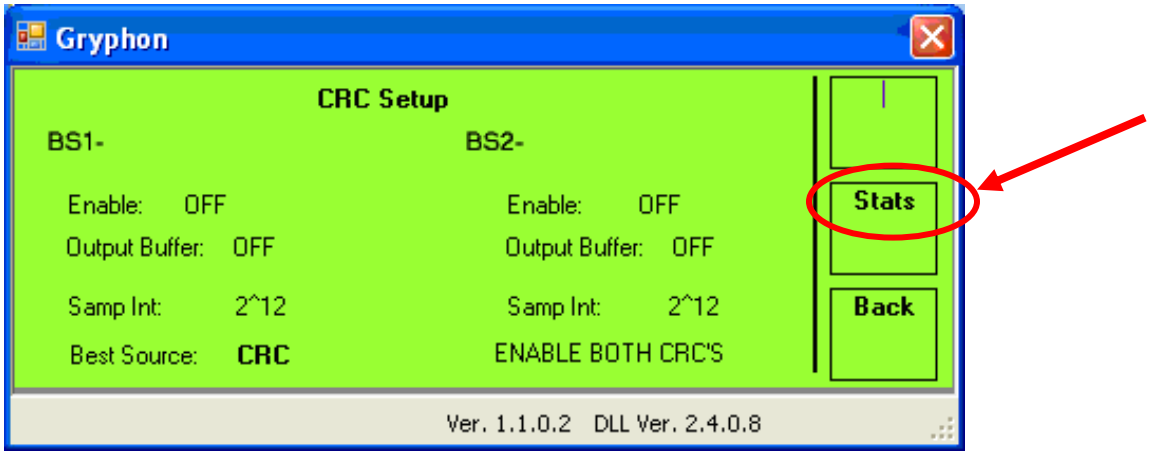


Figure 42 - Opening CRC Status

The CRC Status Screen will display various readbacks and calculations of each CRC channel. Among these are overall Error Count **(Errors)**, overall Minor Frame Count **(Minor Frames)**, a Ratio calculation **(Ratio)**, and a Frame Error Rate calculation **(FER)**. Each of the prior is described in detail at the beginning of 5.9 Configuring CRC.

To Reset either channels counters, use the respective Function keys at any time (**F1 – Resets BS1, F2 – Resets BS2**).

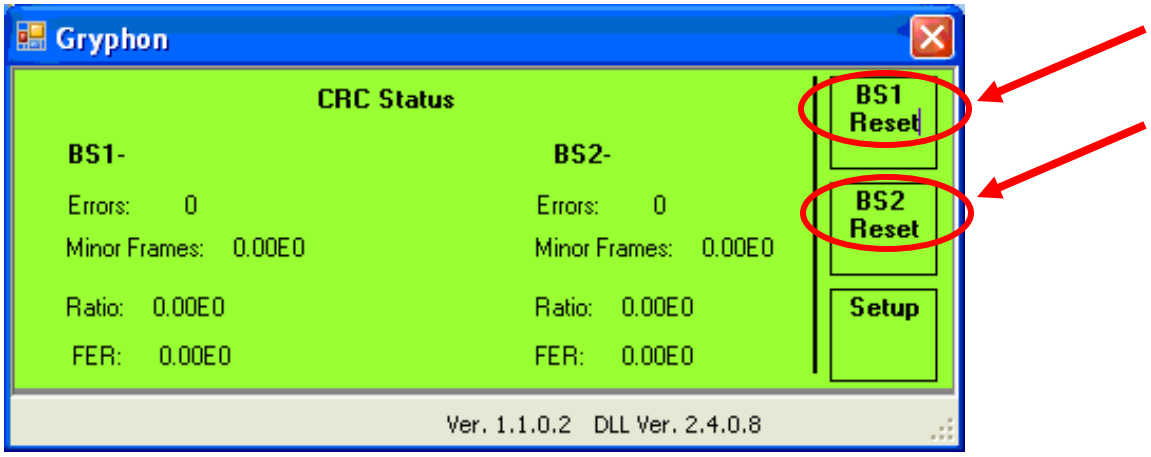


Figure 43 - CRC Status Screen w/ BS Resets

5.10 Configuring Archive

The Gryphon100 unit has the capability to archive frame synched data via the front USB ports to an external memory source. To configure the unit to begin archiving:

1. Select **Archive** from the Main Menu screen.

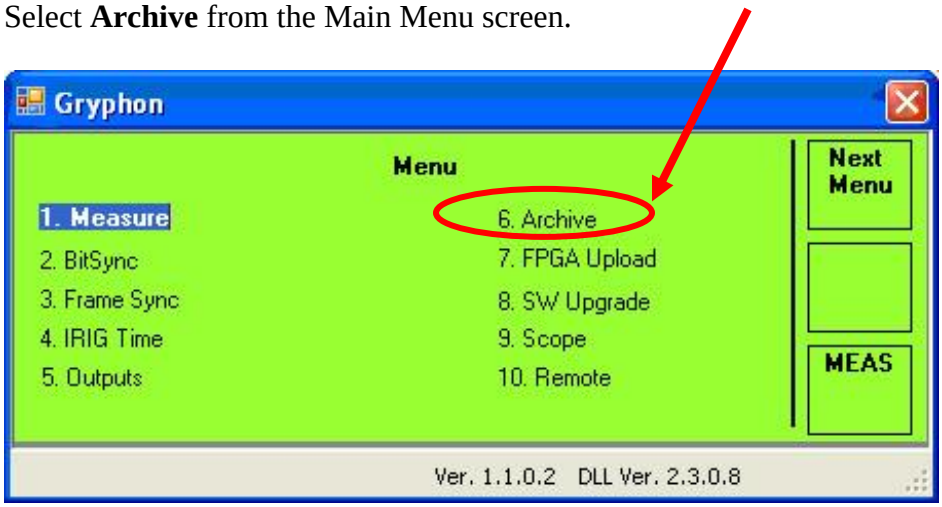


Figure 44 - Main Menu Archive

2. Next choose to enable any or all of the available Frame Syncs of the system. Choose a separate USB drive for each channel to avoid data loss. Although the USB2.0 ports provide over 480 MB of bandwidth in file transfer, the technology of flash memory has not reached this level. We recommend OCZ Rally2 flash drives (see section 5.5.1 for USB specifications).

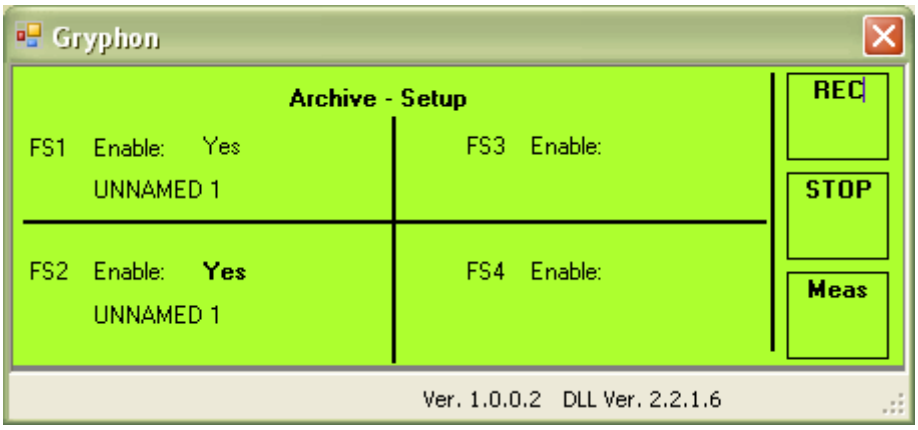


Figure 45 - Archive Setup

3. Press **F1 Rec** to begin archiving all enabled streams.

Channels must have frame lock to archive data to disk unless Data In Search mode is enabled on the frame sync setup.

5.10.1 USB Recommended Specifications

Archiving data via the USB port can require large amounts of available memory and fast write speeds. Below is a table of recommended USB flash drive specifications. Testing was performed using OCZ Rally2 16GB flash drives.

USB 2.0 Certified	Note: Front USB ports are USB 2.0 capable
>16 GB of memory	Note: Memory requirements vary with bitrate and archive length.
True Plug and Play	Note: Compatibility with Windows XP Embedded needed
8-15 MB/s write speeds	Note: Write speeds vary during use. Aim for faster than needed to avoid loss of data.
32-35 MB/s read speeds	Note: Read speeds typically run higher than write speeds.
Illuminating LED to confirm write/read finished	Note: Removing USB drive during a write cycle can lead to loss of data or corrupt memory rendering the drive useless.

Table 3 - Recommended USB Specifications

5.11 Importing and Exporting Configuration Files

The Gryphon100 can import and export locally saved configuration files. To use this feature, first insert a USB device containing a folder titled “Gryphon Configs” in the root directory.

Do Not load configuration files for Gryphon102 onto a Gryphon104 or vice/versa.

1. Open Extended Menu screen (select Menu >> F1 Next).

2. From the extended menu screen select **Import/Export Files** by highlighting the item and hitting OK or simply hitting the number 6.

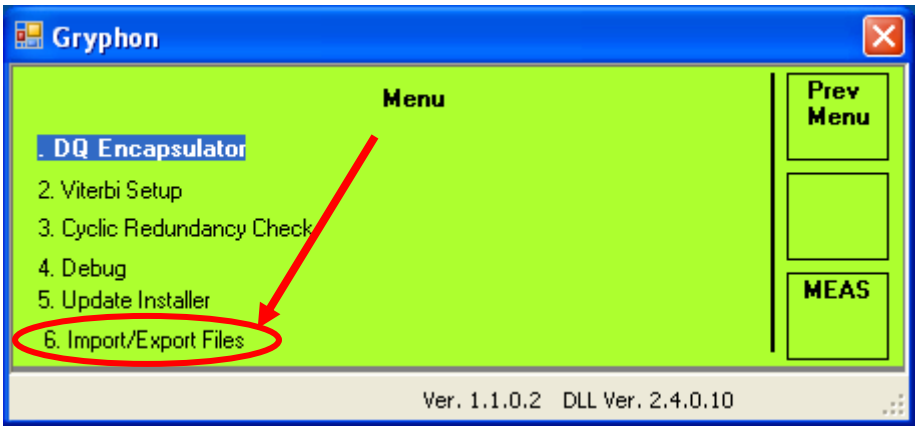


Figure 46 - Extended Menu Screen

3. From the **Import/Export Configurations** screen and with a USB device inserted, select whether you wish to **Import** (load all files contained within *USB:\\Gryphon Configs* folder to Gryphon unit) or **Export** (load all files saved on Gryphon unit to the *USB:\\Gryphon Configs* folder. Select **F1** for Import or **F2** for Export.

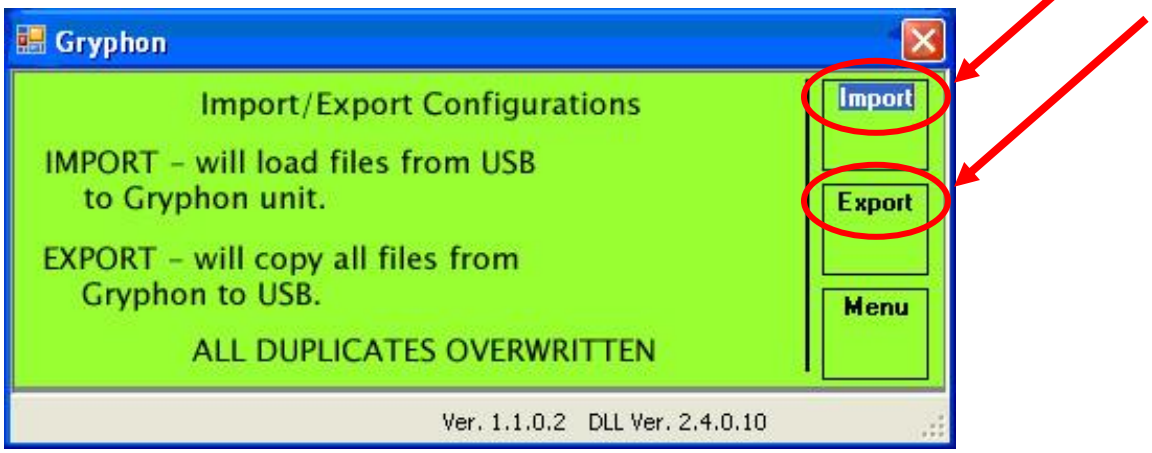


Figure 47 - Import/Export Configurations Screen

Any files of the same name will be overwritten in the destination folder (USB or Gryphon unit).

4. If no errors occur, a message will indicate the process completed. If any errors occur a message will indicate what happened and you can immediately try again.

Chapter 6 RBF Programming

The Gryphon100 products are based on the latest advances in Altera FPGA technology with the latest data acquisition integrated circuits which creates a very versatile telemetry processor unit. The internal hardware can perform many different unique data acquisition and telemetry processing functions including dual full digitally implemented Bit Syncs, PCM Decoms, multi-channel clock data recovery (CDR) modules, SGLS modulator/demodulator and many other data acquisition applications. The basis for the card is three 14-bit analog to digital paths into over 3 million gates of user configurable space. The configurable space is made up of one Altera FPGA.

6.1 Programming

- To program the FPGA's, connect a USB Flashdrive to the Gryphon100.
  a. This drive must contain the "**Gryphon Firmware**" folder in the root directory, which must also contain the two desired firmware files (ex. FPGA63.rbf and FPGA64.rbf). These are provided by the factory.
  **The latest Gryphon firmware is available on www.ulyssix.com
- From the main menu select "FPGA Upload" option 6. This can be done by depressing the number 6 or by the using the appropriate arrow keys until "FPGA Upload" is highlighted and then pressing **OK**.

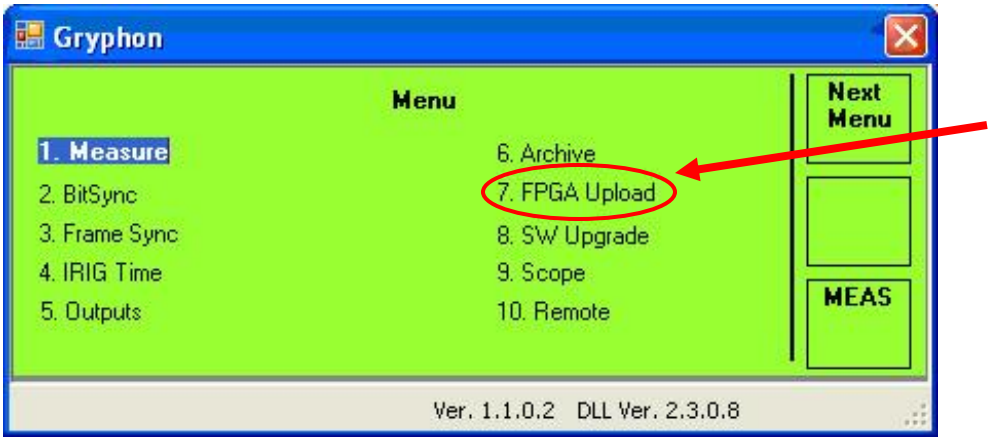


Figure 48 - Main Menu Screen Display

- To load the new firmware press the **F1** "PROG" key and wait for the firmware to load.
  a. While the file is transferring be sure to verify the sum check matches the readme.txt file included with the firmware or located on the web.

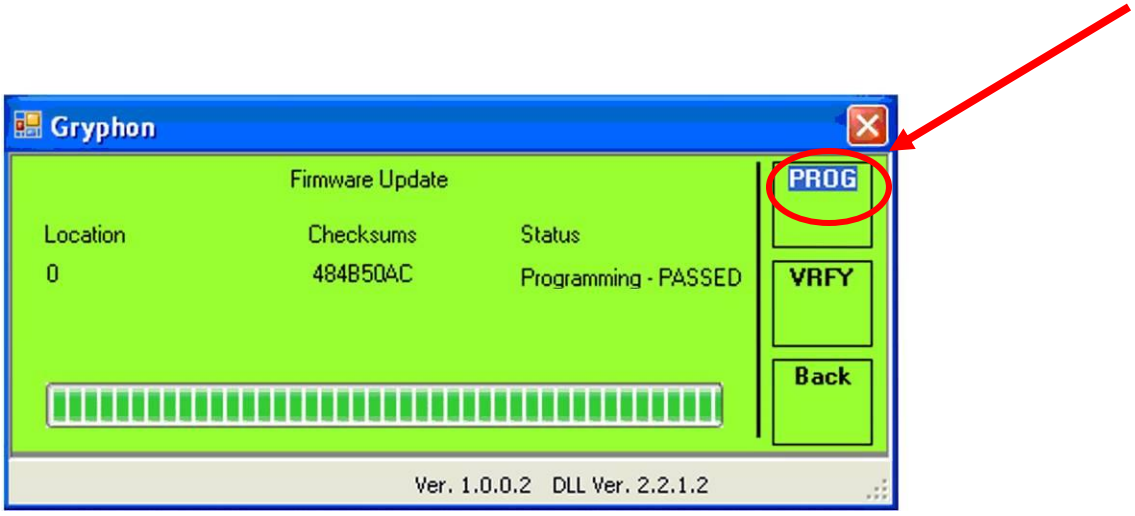


Figure 49 - Firmware Upload Status Screen Display

- Please Note if you see this screen:

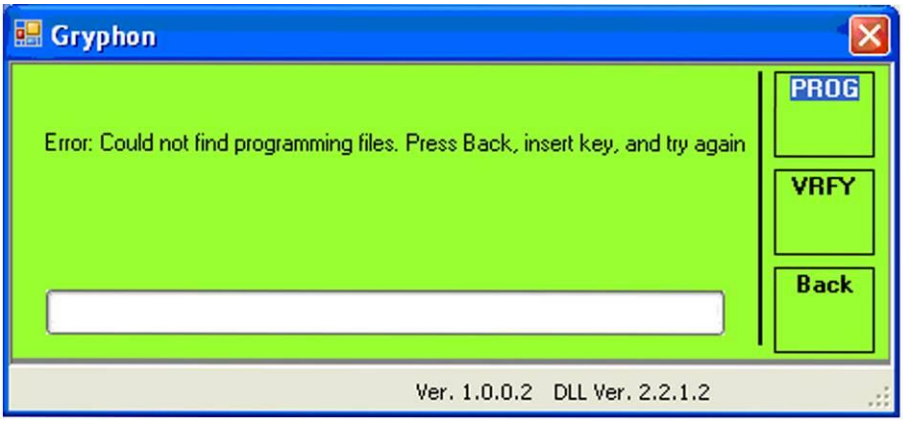


Figure 50 - Firmware Error Screen Display

a. Meaning that there is not a "TarsusPCM Firmware" folder on the USB Flashdrive or that there is an incorrect .rbf file inside that folder.

6.1 Verifying

- To verify the FPGA's, select the "FPGA Upload" option on Main Menu.
- Select the **F2** key labeled "VRFY":

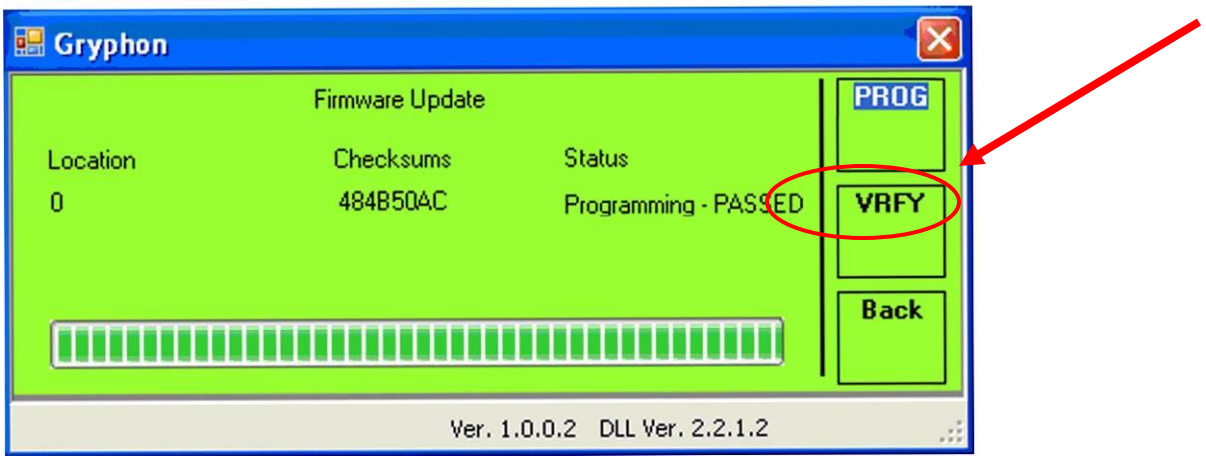


Figure 51 - Firmware Verify Status Screen Display

- This process of verifying is checking to make sure that the firmware that is loaded onto the hardware is the same as the firmware that is on the USB Flashdrive. ** It is not necessary to Verify after each FPGA programming.

Chapter 7 REMOTE SETUP

Remote Setup uses the Gryphon100 RS232 or Ethernet port. Remote setup consists of sending ASCII commands to one of the Gryphon100 I/O ports and receiving responses.

7.1 Remote Configuration

Before sending setup commands, you must configure the Gryphon100's settings. To do this select **Remote** from the menu screen (see Chapter 5). Throughout this section we will discuss each of the setup options and how it affects remote configuration.

To configure the TCP remote connection, follow these steps:

1. Select option **Remote** from the Menu screen.

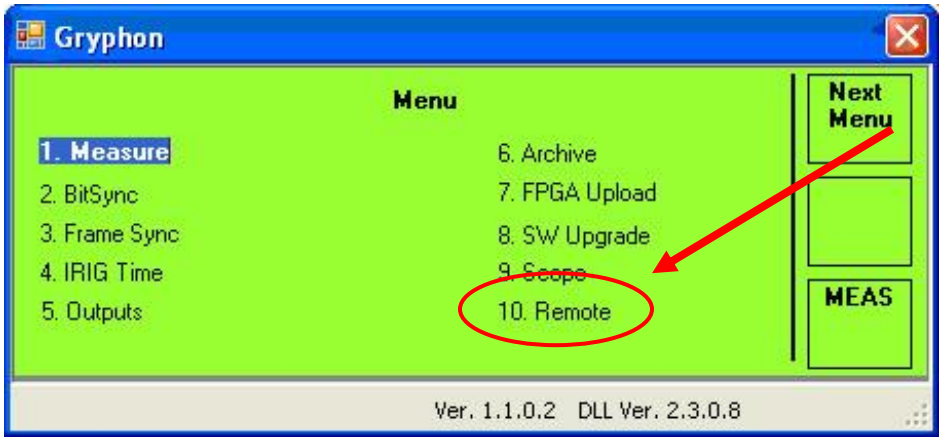


Figure 52 - Menu Screen

2. If configuring the RS232 connection, select RS-232 and move on to step 3. If configuring the TCP/IP select TCP/IP and move to step 4.

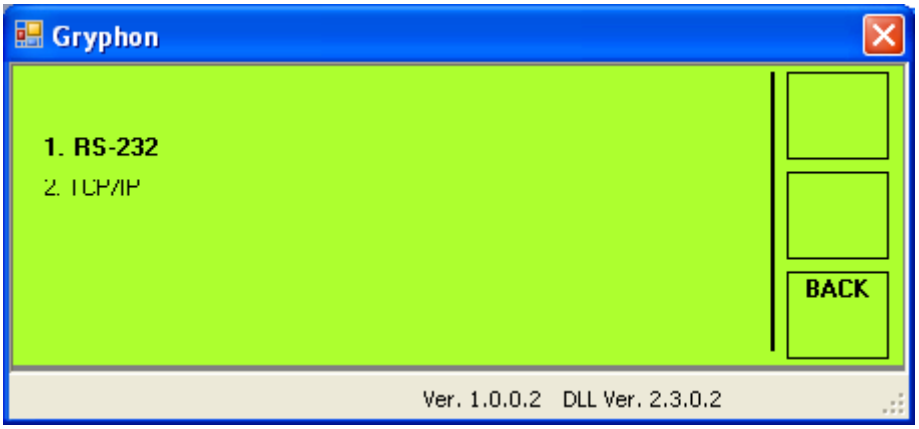


Figure 53 - Remote Menu

3. The RS232 connection allows you to set the Baud Rate, Parity, # Data Bits and Stop Bits. Each can be changed by navigating to the field using the up and down arrow keys and then pan through the options using the right and left arrow keys. Note: these setting must match exactly the settings of the remote computer connecting to the Gryphon.

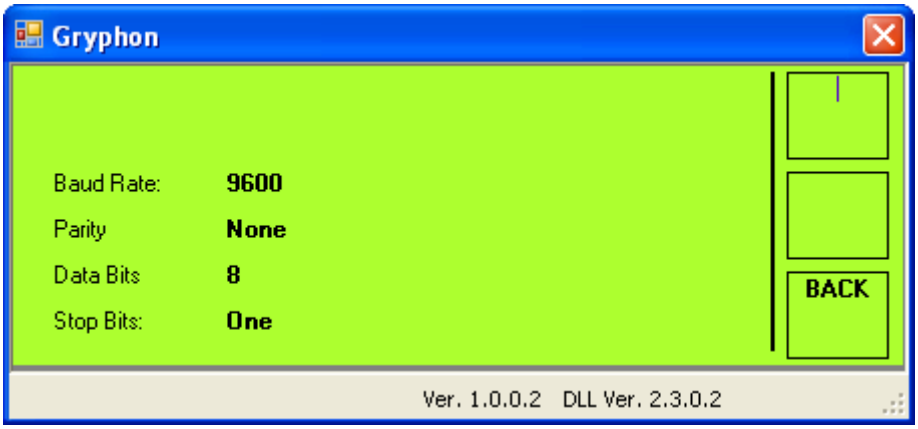


Figure 54 - RS232 Setup Screen

4. The TCP/IP Setup allows for configuration of the internal network card IP address and connecting port number. Enter the IP address using the numeric keypad with decimal point. Enter the Port also using the numeric keypad.

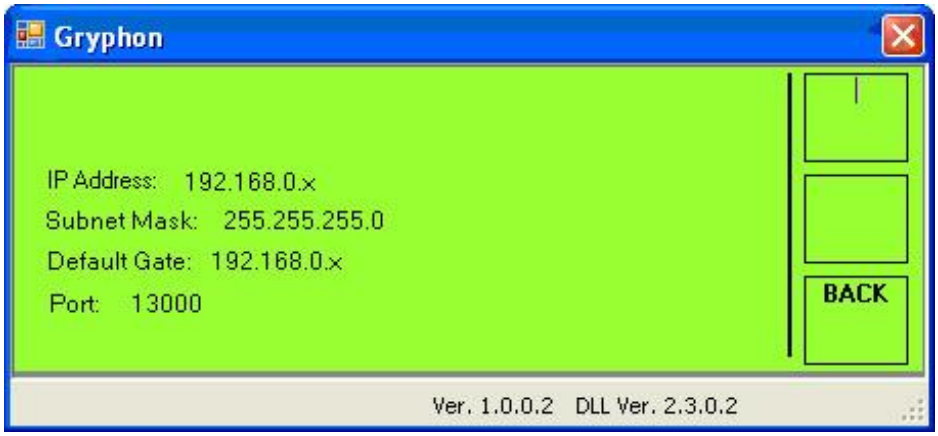


Figure 55 - TCP/IP Setup Screen

7.1.1 TCP/IP

The TCP/IP section on the front panel's Remote Configuration menu allows you to specify the Gryphon100's IP address and mask. For a remote computer to connect to Gryphon100, it must also specify a TCP port. The Gryphon100 listens for connections on port 6001. The Gryphon100's Ethernet port is available at rear panel connector. To connect a remote computer

directly to the Gryphon100's Ethernet port, you must use a cross-over RJ45 cable. If connecting through an Ethernet hub, use a standard RJ45 cable.

The IP address must be unique from all other devices connected to the same network. The mask selects which parts of the address are the network number and which are the host number. A 255 in the mask identifies the corresponding octet in the address as part of the network number.

If you are setting up a simple network consisting of a PC and one or more Gryphon100 units, you can use addresses of the form 192.168.xx.x (where x is a number 1 – 254) and a mask of 255.255.255.0. If you are connecting to an existing network, make sure that the Gryphon100's address has the same network number and mask as the other devices on the network. For example, if the PC that send commands to the Gryphon100 has an address of 192.168.55.2.33 and mask 255.255.255.0, assign the Gryphon100 an address of the form 192.168.55.2.x (x is a number 1 - 254 that is unique on the network) and mask 255.255.255.0. If the network is using DHCP, you must obtain a fixed IP address from the network's administrator.

7.1.2 Serial Port (RS232)

The Gryphon is designed to accept industry standard ASCII commands via the Serial Port. This allows for remote setup and operation of the unit.

The Serial Port setup section of the Remote Configuration allows you to set the Baud Rate, Parity, number of data bits and stop bits. It is imperative that the setup of the Gryphon100 match the setup of the computer remotely connected. The Gryphon100's serial port (male DB9 connector) is available on the real panel connector. To connect a remote computer to the Gryphon100's serial port, you must use a crossover cable or a null modem cable—the receive and transmit signals (lines 2 and 3) must be crossed.

7.1.2.1 Echo

The Echo option controls whether the Gryphon100 echoes its input characters back to the remote computer, and the type of response the Gryphon100 makes after processing a command.

When Echo is enabled, the Gryphon100 echoes each character as it is received. When a complete line is received (terminated by newline character, <nl> (hex 0A), or carriage return, <cr> (hex 0D), the termination character is echoed and the command is then processed. If an error occurs while processing the line, the Gryphon100 sends an error message that starts with "ERROR:". This mode is designed for when a user is typing the commands from a remote terminal, such as a PC running the HyperTerminal program under the Windows operating system.

When Echo is disabled, the Gryphon100 makes no reply until it has received and processed an entire line. The response is a single character: an <ack> (hex 06) for an accepted line, or a

<bel> (hex 07) for an error. No error message is returned. Blank lines are ignored; neither <ack> nor <bel> is sent. This mode is designed for when the commands are sent from an automated program running on the remote computer, such as the Gryphon100 Bit Sync Menu.

7.1.2.2 EOT

EOT determines whether the Gryphon100 will send an end-of-transmission character, <eot> (hex 04), at the end of its responses. Enabling EOT is useful when writing client software because it allows you to detect the end of a response independent of whether the response is a single line or multiple lines. This may be helpful when programming some software communications libraries, such as network sockets.

When EOT is enabled, each response is terminated with an <eot> (hex 04) character, allowing you to detect the end of single and multi-line responses in a uniform way. When both Echo mode and EOT mode are enabled, the last response line ends with <cr><nl><eot>. With Echo disabled but EOT enabled, the last response line ends with <bel> or <ack> followed by <eot>.

7.1.3 Remote Interface Description

Remote setup of the Gryphon100 is done through a specified set of ASCII commands for both TCP/IP and RS232 connections. This section will focus on the protocol of the commands/programs that setup and operate the Gryphon100. Many of the mentioned commands are based on industry standards, however, many are unique features of Ulyssix and the Gryphon100.

All commands are case-insensitive ASCII and must be terminated by a newline character, <nl> (hex 0A), or a carriage return, <cr> (hex 0D). The setup should be sent a line at a time. Before sending another line, the remote client should wait for the echo of the complete line when Echo is enabled, or the <ack> (hex 06) or <bel> (hex 07) when Echo is disabled. In no-Echo mode, blank lines are ignored; neither <ack> nor <bel> is sent.

Commands can be a single line, meaning, BITS 1 STATUS asking, “What is the lock status of bit sync 1?” or can be an entire program setting up many features sequentially before terminating. Typically, single line commands are used to ask a quick question of the Gryphon100, while command programs are intended to setup the individual pieces of hardware.

After receiving a complete line, the Gryphon100 makes a response that can be affected by both the Echo and EOT modes. If Echo is enabled, all response lines are terminated by <cr><nl>. Error lines start with "ERROR:" followed by the error message. In EOT mode, each response is terminated with an <eot> (hex 04) character, allowing you to detect the end of single and multi-line line responses in a uniform way. When both Echo mode and EOT mode are enabled, the last response line ends with <cr><nl><eot>. When Echo is disabled, some Single Line Commands still generate a response line, in addition to the <bel> or <ack>. The last response line is terminated by <cr><nl> followed by the <bel> or <ack>. With Echo off and EOT on,

the last response line is terminated with <cr><nl> followed by <bel> or <ack>, followed by <eot>.

The following lists the Gryphon100's special handling of some characters.

Code	Hex	CTRL	Action
<enq>	05	^E	Returns the remote status of the unit. In echo mode, response is REMOTE<nl> or LOCAL<nl>. In no-echo mode, response is<GS> (hex 1D) for remote, <FS> (hex 1C) for local. Note: Gryphon100 always responds REMOTE—command is for software compatibility with the Gryphon100.
<bs>	08	^H	Backspaces one character.
<nl>	0A	^J	Terminates a line.
<cr>	0D	^M	Terminates a line.
<dc2>	12	^R	Turns off Echo mode.
<dc4>	14	^T	Turns on Echo mode.
<del>	7F, C3	--	Deletes the line.
<so>	0E	^N	Turns on EOT mode.
<si>	0F	^O	Turn off EOT mode.

Table 4 - Remote Setup Special Characters

7.2 Single Line Commands

Single-line commands are commands that cannot be embedded in a setup program. They are used to invoke an action or request a response. In these commands, n = 1, 2, 3 or 4 referring to channels 1, 2, 3, and 4 (if the unit is a dual channel system, only 1 and 2 will apply).

7.2.1 Software Version

Get the Gryphon100 front panel software revision with the command

VERSION

The response string has the form:

Vers *vers_no date* Gryphon10*n*

Where *vers_no* is the version number, *date* is the release date, and Gryphon10*n* will determine the model of the unit (n=2 or 4 depending on model).

7.2.2 Self-Test

Use the following command to determine if the Bit sync is in functional order. This test will perform a quick diagnostic to determine if the bit sync is responding to commands.

BITS n TEST

The response is PASS for functioning bit sync, FAIL for a bit sync that should not be used.

7.2.3 Retrieve Setup

To retrieve the setup of a bit sync, use:

BITS n SETUP

The response is multiple lines, the first being BITS n followed by lines reporting the current setup of the card, with the final line being END. The setup is described using the same syntax as would be used to program it.

7.2.4 Bit Sync Lock Status

To query the lock status of the bit sync, use:

BITS n STATUS

The response is LOCK or SEARCH.

7.2.5 Single Line Commands Summary

Command	Response
VERSION	'VERS *vers_no date* Gryphon10*n*' *n*=2 or 4 representing number of channels
BITS *n* TEST *n*=channel being tested	'PASS' or 'FAIL'
BITS *n* STATUS *n*=channel status requested for	'LOCK' or 'LOSS'
FSYN *n* STATUS *n*=channel status requested for	'LOCK', 'CHECK' or 'SEARCH'
SUBFSYN *n* STATUS *n*=channel status requested for	'LOCK', 'CHECK' or 'SEARCH'

Table 5 - Single Line Command Summary Table

7.2.6 Setup Programs

A setup program is used to setup any or all parts of the hardware. It begins with a specification of what channel is being setup (ex: "BITS 1" would indicate channel one) and ends with the command END. A setup program spans multiple lines. No Single Line commands can be issued in the middle of a Setup Program. The general form of a Gryphon100 setup program is:

BITS n
.
.
.
commands
.
.
.
END

where n must be 1, 2, 3 or 4 to address Channel 1, 2 3, 4. The END statement finishes the programming by checking the setup for errors, and if there are none, downloading the setup to the addressed card. The remaining subsections describe the commands that can be placed in a Setup Program.

7.2.7 Bit Sync Source Select

Select the decoder input source using the command

SRC=*n*

where *n* is one of the following values:

1 – Bit Sync input 1 (single ended)
2 – Bit Sync input 2 (single ended)
3 – Bit Sync input 3 (single ended)
4 – Bit Sync input 4 (differential)

7.2.8 Source Termination

To select the input source termination, you can use the command:

TERM *n*

n= the desired termination value. Choose from the following:
50 – 50Ω (Ohm) termination
75 – 75Ω (Ohm) termination

LO – 75Ω (Ohm) termination
10K – 10KΩ (Ohm) termination
HI – 10KΩ (Ohm) termination

7.2.9 Decoder Input Codes:

Specify the input code type you are going to process by entering the mnemonic as shown below in the Command column.

IRIG Code	Command	Code Definition
NRZ-L	NZL	Non-Return-to-Zero Level
NRZ-M	NZM	Non-Return-to-Zero Mark
NRZ-S	NZS	Non-Return-to-Zero Space
BiP-L	BPL	Bi-phase Level (Split Phase)
BiP-M	BPM	Bi-phase Mark
BiP-S	BPS	Bi-phase Space
RZ	RZ	Return-to-Zero
RNRZ-L	RNZ-n	Randomized Non-Return-to-Zero Level

When a randomized code type is selected, the derandomizer will be automatically engaged. *n* must be specified to set the size of the shift register. If the code type is not randomized, no *n* needs to be specified.

Command Format:
code n

n = (11 or 15)

7.2.10 Derandomizer Pattern Direction

Set the direction of the PN pattern applied by the derandomizer using one of the following commands:

FOR *Derandomize forward PN patterns*
REV *Derandomize reverse PN patterns*

Use this command along with the input code command (section 6.4.3) to decode randomized data. The input code command selects the PCM code and run length, and this command sets the direction of the PN pattern. For example, to decode NRZ-L randomized with a PN11R pattern, use the commands

RNZ 11
REV

7.2.11 Bit Rate

Set the bit rate with the command

BR=rate

The Gryphon100 accepts bit rates anywhere between 1 bps and 32 Mbps

The following are all valid commands for setting a bit rate of 1.2 Mbps.

BR=1.2E6
BR=1200000
BR=1200K
BR=1.2M

7.2.12 Loop Width

Loop width controls the Bit Syncs PLL's capture range. In general, use a smaller loop width for noisy, frequency stable signals, and a larger loop width for signals that may have Doppler effects or be subject to tape speed variations.

Set the loop width with the command

LW=*n.nn%*

The loop width can be set from 0.01% to 3.0% with a resolution of 0.01%. No % sign needs to be transmitted, it is assumed.

7.2.13 Loop Tracking

Loop tracking sets the maximum allowable PLL frequency deviation from the programmed bit rate. The larger the numeric value of the loop tracking parameter, the larger the range.

The command

TRK=*n.nn%*

The tracking range can be set between 0.01% and 3.00% of the bit rate. No % sign needs to be transmitted, it is assumed.

7.2.14 Bit Sync Input Polarity

Each bit sync input polarity can be declared by using the command:

[src] [pol] [src]=IDAT or XDAT depending whether the data is being bit synced, or going directly to the frame sync respectively.
[pol]= NOR or INV depending whether the polarity of the data is normal or inverted respectively.

7.2.15 Bit Sync Outputs

Each bit sync has 3 independent outputs. The first 2 are TTL level clock and data outputs and the third is a bipolar data output. Each output is independently programmable. For outputs 1 and 2 the code type, clock phase and polarity are selectable. For the third output code type and polarity are selectable. Use the following commands to program each.

Output1 (TTL level clock and data)

OUT= *[code] [n] [direction]*
[code]= any of the input code types described in section 7.2.20
[n]= shift register size of derandomizer (left blank if data is not randomized)
[direction]= FOR or REV for direction of derandomizer (left blank if data is not randomized)
CLK *[y]*

where y is 0, 90, 180, or 270, expressing the phase shift in degrees between the start of the data bit interval and the positive transition of the output clock.

Polarity
[n]

Where n is NOR or INV depending on whether the data should be output in normal or inverted polarity.

Output2 (TTL level clock and data)

CODE or OUTPUT2 *[code] [n] [direction] [polarity]* CLK *[y]*

[code]= any of the input code types described in section 7.2.20
[n]= shift register size of derandomizer (left blank if data is not randomized)
[direction]= FOR or REV for direction of derandomizer (left blank if data is not randomized)
[polarity]= NOR or INV corresponding to normal or inverted data.
[y]= 0, 90, 180, 270 corresponding to the degree shift between data and clock

Output3 or TAPE Out (Bipolar data)

TAPE or OUTPUT3 *[code] [n] [direction] [polarity]*

[code]= any of the input code types described in section 7.2.20

[n]= shift register size of derandomizer (left blank if data is not randomized)
[direction]= FOR or REV for direction of derandomizer (left blank if data is not randomized)
[polarity]= NOR or INV corresponding to normal or inverted data.

7.2.16 Decoder Data Polarity

The following two input polarity commands are available:

NOR selects NORMAL polarity
INV selects INVERTED polarity

7.2.17 AGC Freeze

Each Bit Sync can lock the Auto Gain Control values at any given moment. Typically, this would be done when the incoming signal is of steady level and offset. Enabling AGC Freeze will increase the resync acquisition speed in this situation. AGC Freeze will also increase the bit syncs tolerance of long streams of '1's and '0's in a Non-Return to Zero stream.

To enable or disable AGC Freeze use the following commands:

AGCFREEZE (enables AGC Freeze)
NOAGCFREEZE (disables AGC Freeze)

7.2.18 Frame Synchronizer

Each bit sync in the Gryphon100 has an accompanying Frame Synchronizer and Sub Frame Synchronizer. To setup the Frame Sync use the following commands (all on single line).

FMT FRAME *[commands]*
or
FSYN *[commands]*

The following are all commands available for the frame sync setup.

MINFRM=*[n]*
[n] = Number of minor frames in the major frame

LEN=*[n]*
[n] = Number of bits in minor frame

SYNCBITS=*[n]*

[n] = Number of bits in frame sync pattern. The Sync pattern will be set to the IRIG standard of length n.

SYNC=*[n]*

[n] = Frame sync pattern

MASK=*[n]*

[n] = Frame sync mask. Any 1 in a bit location will tell the frame sync to ignore that bit of the pattern

SYNCERRS=*[n]*

[n] = Number of allowed frame sync bit errors

SLIP=*[n]*

[n] = Number of allowed bit slips. The command SLIP will indicate 1 allowed bit slip. *[n]* can be any number up to ½ the minor frame size.

NOSLIP

Turns off allowed bit slips

AUTO

Turns ON Auto Polarity. Without frame lock, the polarity will flip until lock is acquired

NOAUTO

Turns OFF Auto Polarity.

CHECK=*[n]*

[n] = number of frame sync patterns seen before frame sync status moves from 'Search' to 'Check'

LOCK=*[n]*

[n] = number of frame sync patterns seen before frame sync status moves from 'Check' to 'Lock'

SEARCH=*[n]*

[n] = number of frame sync patterns seen before frame sync status moves from 'Check' to 'Search'

LOCKTOCHECK=*[n]*

[n] = number of frame sync patterns seen before frame sync status moves from 'Lock' to 'Check'

BURST

Turns ON Burst Mode. Will immediately put the frame sync status to 'Lock' upon seeing 1 frame sync pattern. This eliminates losing the first minor frame of data.

NOBURST

Turns OFF Burst Mode

DIS

Turns ON Data In Search Mode. Will continue to archive data upon loss of frame sync 'Lock'.

NODIS

Turns OFF Data in Search Mode

Any or all of the commands may be used to program the frame sync. All should be located on a single line with a Line Feed or Carriage Return only at the end. The BITS n command at the beginning of the setup program indicates which frame sync is setup.

7.2.19 Sub Frame Synchronizer

Each frame sync in the Gryphon100 has an accompanying Sub Frame Synchronizer. To setup the Sub Frame Sync use the following commands (all on single line).

SUBFSYN *[commands]*

The following are all commands available for the sub frame sync setup.

[type]

[type] = NONE, SFID, or FCC depending on type of sub frame sync in frame

LOCATION=*[n]*

[n] = Number of bits from end of Frame Sync pattern to end of Sub Frame Sync

NUMSFIDBITS=*[n]*

[n] = Number of bits in sub frame sync word

STARTVAL=*[n]*

[n] = Value of SFID word in first minor frame

ENDVAL=*[n]*

[n] = Value of SFID word in last minor frame

CHECK=*[n]*

[n] = number of correct sub frame sync words seen before sub frame sync status moves from 'Search' to 'Check'

LOCK=*[n]*

[n] = number of correct sub frame sync words seen before sub frame sync status moves from 'Check' to 'Lock'

SEARCH=*[n]*

[n] = number of correct sub frame sync words seen before sub frame sync status moves from 'Check' to 'Search'

LOCKTOCHECK=*[n]*

[n] = number of correct sub frame sync words seen before sub frame sync status moves from 'Lock' to 'Check'

[wordorder]

[wordorder] = MSB or LSB specifying the order bits are transmitted in the stream

Any or all of the commands may be used to program the sub frame sync. All should be located on a single line with a Line Feed or Carriage Return only at the end. The BITS n command at the beginning of the setup program indicates which sub frame sync is setup.

7.2.20 Setup Program Summary

Command	**Description**	**Example**
BITS n	Begins setup program and indicates channel being setup n = 1, 2, 3, or 4 depending on channel being setup	BITS 2<cr><nl>
END	Ends setup program	END<cr><nl>
Bit Sync Setup Commands	**Description**	
SRC=n	Selects input data source n = 1, 2, 3, or 4 corresponding to 1 of 4 inputs per bit sync	SRC=3<cr><nl>
BR=n	Sets input bit rate from 1 bps to 32 Mbps n = bit rate	BR=1.2E6<cr><nl>
[code] [n]	Sets the input code type. n = shift register size if randomized code type.	RNZ 11<cr><nl> or BPL<cr><nl>
TERM=n	Sets input impedance. n = 50, 75 or LO, 10K or HI	TERM=HI<cr><nl>
[direction]	Sets derandomizer direction. FOR or REV	REV<cr><nl>
[src] [pol]	Sets input src (IDAT or XDAT) and input polarity (NOR or INV)	IDAT INV<cr><nl>
[polarity]	Sets output polarity to normal (NOR) or inverted(INV)	NOR<cr><nl>
LW=n	Sets loop bandwidth percentage. n = 0.01 to 3.00	LW=0.5<cr><nl>
TRK=n	Sets tracking range percentage. n = 0.01 to 3.00	TRK=0.10<cr><nl>
AGCFREEZE	Enables AGC Freeze mode	AGCFREEZE<cr><nl>
NOAGCFREEZE	Disables AGC Freeze mode	NOAGCFREEZE<cr><nl>
OUT= [code] [n] [dir]	Sets Output 1 to specified code type	OUT RNZ 15 REV<cr><nl>

CLK n	Sets Output 1 Clock phase to n. n = 0, 90, 180, or 270	CLK 180<cr><nl>
OUTPOL n	Sets Output 1 Polarity to n. n = NOR or INV	OUTPOL NOR<cr><nl>
OUTPUT2 [code] [n] [dir] [pol] [clk]	Sets Output 2 code type, clock phase and polarity	OUTPUT2 BPL INV 90<cr><nl>
TAPE [code] [n] [dir] [pol]	Sets Output 3 or Tape out code type and polarity	TAPE NZL NOR<cr><nl>
Frame Sync Setup Commands	**Description**	**Example**
FSYN [commands…]	Indicates beginning of Frame Sync setup line	FSYN …….<cr><nl>
MINFRM=n	Sets major frame size. n = number of minor frames in major frame	MINFRM=32
LEN=n	Sets length of minor frame. n = number of bits in minor frame	LEN=2047
SYNCBITS=n	Sets number of bits in frame sync pattern. n = bits in pattern	SYNCBITS=32
SYNC=n	Sets frame sync pattern. n = sync pattern in hex	SYNC=FE6B2840
MASK=n	Sets sync mask n = sync mask pattern in hex	MASK=00000001
SYNCERRS=n	Sets number of errors allowed in frame sync pattern. n = number of errors allowed	SYNCERRS=3
SLIP=n	Sets number of bits frame sync location can be off. n = bit slips allowed	SLIP=45
NOSLIP	Sets bit slips to zero	NOSLIP
AUTO	Enables Auto Polarity mode	AUTO
NOAUTO	Disables Auto Polarity mode	NOAUTO
CHECK=n	Sets number of frame sync patterns to move from ‘Search’ to ‘Check’ status. n = number of patterns	CHECK=1
LOCK=n	Sets number of frame sync patterns to move from ‘Check’ to ‘Lock’ status. n = number of patterns	LOCK=2
SEARCH=n	Sets number of frame sync patterns to move from ‘Check’ to ‘Search’ status. n = number of patterns	SEARCH=3
LOCKTOCHECK=n	Sets number of frame sync patterns to move from ‘Lock’ to ‘Check’ status. n = number of patterns	LOCKTOCHECK=1
BURST	Enables Burst mode	BURST
NOBURST	Disables Burst mode	NOBURST
DIS	Enables Data In Search mode	DIS
NODIS	Disables Data In Search mode	NODIS
Sub Frame Sync Setup Commands	**Description**	**Example**
SUBFSYN [commands]	Indicates beginning of Sub Frame Sync setup line	SUBFSYN ……<cr><nl>
[type]	Indicates type of sub frame sync either NONE, SFID, or FCC	SFID
LOCATION=n	Sets location of SFID word. n = number of bits from end of frame sync pattern to end of SFID word	LOCATION=16

NUMSFIDBITS=n	Sets size of SFID word. n = number of bits in SFID word	NUMSFIDBITS=16
STARTVAL=n	Sets value of SFID word in first minor frame. n = beginning count value	STARTVAL=0
ENDVAL=n	Sets value of SFID word in last minor frame. n = ending count value	ENDVAL=31
CHECK=n	Sets number of correct sub frame sync words to move from 'Search' to 'Check' status. n = number of minor frames	CHECK=1
LOCK=n	Sets number of correct sub frame sync words to move from 'Check' to 'Lock' status. n = number of minor frames	LOCK=2
SEARCH=n	Sets number of correct sub frame sync words to move from 'Check' to 'Search' status. n = number of minor frames	SEARCH=3
LOCKTOCHECK=n	Sets number of correct sub frame sync words to move from 'Lock' to 'Check' status. n = number of minor frames	LOCKTOCHECK=1
[wordorder]	Sets the order of bits in SFID to either MSB (most significant bit first) or LSB (least significant bit first)	MSB

Table 6 - Program Summary Table

7.2.21 Default Values

To revert to default values for all parameters, use the following command:
INIT

The parameter default values are listed below.

Source Select	1
Source Termination	LO for all inputs
Input Code	NZL
Derandomizer	OFF
Derand Direction	FOR (forward)
Bit Rate	1000000
Loop Width	0.1%
Loop Tracking	0.1%
Decoder Clock Phase	0 (degrees)
Decoder Data Polarity	NOR (normal)
Randomizer	0 (pass through)
Rand Direction	RFOR (forward)
TAPE Output	NZL (NRZ-L)
CODE Output	DATA (encoder output)
FSYN	OFF
BERT	OFF

References

[1] Telemetry Standards, IRIG STANDARD 106-04 Part I, Secretariat, Range Commanders Council, White Sands Missile Range, Mew Mexico. **http://jcs.mil/RCC**

Chapter 8 Software Upgrade

To access the Gryphon122 Software Upgrade screen, select the number **6** key from the Menu screen or use the Arrow keys and then select OK.

Figure 56 - Software Upgrade

The software upgrade screen displays the current version of the software, release date and model of the product. The internet MAC address is also displayed for ease in setting up the Ethernet interface.

To perform the software upgrade, go to the Ulyssix web site and login into the Gryphon section to get the latest Gryphon122 software. The files need to be loaded onto a USB drive in a **Gryphon Upgrade** folder on the USB drive. By hitting the **F1 UPDT** key, the Gryphon122 will automatically copy the new files that are on the USB drive onto the Gryphon122 and restart the system.

Chapter 9 Troubleshooting

1. **No Bit Lock** – Diagnosing bit lock can be very difficult. First ensure data is making to the hardware by viewing the Eye Pattern on the Measure screen. If there is a flat line, you will need to double check the rear input selection and the cabling being used. If data is making it to the board and still no Bit Lock, re-verify the bit rate and code type selections. Lastly check an alternative Bit Sync using the same data source before calling the factory for assistance.

2. **No Frame Sync Lock** – After verifying good bit lock by viewing the Eye Pattern on the Measure screen, first attempt enabling Auto Polarity on the Frame Sync Setup screen to check for an inverted data stream. Next attempt adding bit slips up to half the size of a minor frame. This will open the window of tolerance for finding a Frame Sync pattern. Next attempt allowing for Sync Errors. Lastly verify with another Frame Sync using the same data stream before calling the factory for assistance.

3. **Screen Errors** – Communication to the front LCD display is accomplished internally using RS232. With that comes the possibility of interrupting a command with a second command. This may be seen when large amounts of data is written to the LCD such as loading a screen. If a second button is hit prior to the screen being loaded, this command will cause an interruption in the screen. It is important to understand that underneath all operations are continuing without any problems, but the screen was written incorrectly. To fix, refresh the screen allowing 1 second to load.

4. **Format File Not Saved** – The Gryphon architecture uses an embedded operating image to load quickly and consistently. During each session data is saved to DRAM and not converted to the operating image until the next proper shutdown. If power is lost abruptly the system will reboot to the last saved image which was formed during the last proper shutdown. It is important to periodically shutdown after adding format files or changing software.

5. **Gryphon Hangs During SW Update** – If the Gryphon freezes and becomes unresponsive during a software update using a USB drive, first remove the USB, then hold the front power rocker switch until the unit powers off. Check the file system of your USB and ensure that it is formatted to FAT32 or exFAT and not NTFS. If this does not solve the problem, please contact the factory for further instructions.

Chapter 10 USB Device Settings

10.1 USB Folders

The Gryphon100 unit allows for input and output of data, files, and configurations via the front USB ports. The unit needs to find specific folders in the root of the USB device for certain functions.

Folder Name	Function	Contents
Gryphon Upgrade	Input -- Used when updating the Gryphon100 operating.	All .dlls and .exes the Gryphon needs to function. Provided by factory.
Gryphon Firmware	Input -- Used when updating the firmware of the internal TarsusHS hardware.	2 files – FPGA63.rbf and FPGA64.rbf, readme.txt may also be included. Provided by factory.
Gryphon Archive	Output – Used to stream archive data from the Gryphon unit.	Any files archived. File extension is .tad.
Gryphon Configs	Input/Output – Used to import or export Gryphon configuration files.	Exported files from any Gryphon unit (.xml extension). Can be loaded onto any Gryphon100 unit.

Figure 57 - USB Folder Descriptions

10.2 USB File System

Ulyssix recommends a USB device file format of exFAT. Typical USB drives under 32 GB are formatted in FAT32 file system. This is perfectly acceptable, but FAT32 restricts the maximum file size to ~4 GB. This limitation could become an issue with larger archive files. FAT32 is also not applicable to larger drives sizes, where exFAT is.

NTFS file systems are regarded as not ideal due to the file overhead and possible security flags that would prevent the Gryphon from launching executables. This may be the problem if you attempt to update Gryphon software and the system fails to restart.

For more information on the exFAT file system, please see:
http://msdn.microsoft.com/en-us/library/aa914353.aspx

Chapter 11 Archive Data Files Explained

Archive files recorded by the Gryphon100 binary files containing data from Frame Sync circuitry of the Ulyssix PCM hardware. After Frame synchronizing the data is stuffed into a large dual port memory device. Along with the data, a header is generated and stuffed into the dual port memory at the beginning of every minor frame. The data is read from the dual port memory by the Gryphon100 software and stored to an external memory source via the USB Ports on the front.. Each file stored contains a file header and all minor frame and header data captured during an archive sequence. All archive data files end with the extension ".tad". (Tarsus Archive Data) This section of the manual explains the format of the archive data.

9.1 Data Storage Format

The Gryphon100 stores the archive data in "Little Endian" format. "Little Endian" derived from the phrase "Little End In" means the little end of the data is stored in memory fist. For example, 0x12345678 would be stored in memory as (0x78 0x56 0x34 0x12).

9.2 File Header Definition

Each archived data file contains one file header structure. The file header is stored to indicate the date, time and configuration file used during the archive sequence. All file header data is in ASCII characters to allow viewing with a standard text editor. The header consists of 328 bytes and is defined as follows:

10 bytes – Signature
12 bytes – Version
22 bytes – Date/Time
260 bytes – Configuration file and path
12 bytes – Input Data Source (Either "Frame Sync" or "Decom")
1 Unsigned Integer (32 bits) - Bits/Minor Frame
1 Unsigned Integer (32 bits) - Spare
1 Unsigned Integer (32 bits) – Spare

9.2.1 File Header Example

```
00000000  54 61 72 73 75 73 50 43  4D 00 31 2E 38 2E 32 2E  TarsusPCM.1.8.2.
00000010  32 00 00 00 00 00 32 2F  31 31 2F 32 30 30 35 20  2.....2/11/2005
00000020  31 31 3A 34 39 3A 35 38  20 41 4D 00 43 3A 5C 50  11:49:58 AM.C:\P
00000030  72 6F 67 72 61 6D 20 46  69 6C 65 73 5C 55 6C 79  rogram Files\Uly
00000040  73 73 69 78 5C 54 61 72  73 75 73 50 43 4D 5C 43  ssix\TarsusPCM\C
00000050  6F 6E 66 69 67 75 72 61  74 69 6F 6E 46 69 6C 65  onfigurationFile
00000060  73 5C 64 65 6D 6F 2E 78  6D 6C 00 00 00 00 00 00  s\demo.xml......
00000070  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
00000080  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
00000090  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
000000a0  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
000000b0  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
000000c0  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
000000d0  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
000000e0  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
000000f0  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
00000100  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
00000110  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
00000120  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  ................
00000130  46 72 61 6D 65 53 79 6E  63 00 00 00 00 02 00 00  FrameSync.......
00000140  00 00 00 00 00 00 00 00                           ........
```

File Header Information
Signature = TarsusPCM
Version = 1.7.11.9
Date/Time = 12/28/2004 2:12:25 PM
Configuration File = C:\Program Files\Ulyssix\TarsusPCM\ConfigurationsFiles\demo.xml
Source = Frame Sync

Figure 58 – Archive File Header Example

9.3 Minor Frame Header Definition

As stated above, header data precedes every minor frame in the archive file. The header contains time in Binary Coded Decimal (BCD) along with various status indicators. The header data is defined as three 32 bit data words with the following format.

32 Bit Words	Bits 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0000				100's days				10's days				1's days				10's hours				1's hours				10's minutes				1's minutes			
1	10's seconds				1's seconds				100's msec				10's msec				1's msec				100's usec				10's usec				1's usecs			
2	Minor Frame Count																TC R Err	TC F Err	I/E	Slip	# Sync Errors				B Lock			SF Lock			MF Lock		FFI	

Table 7 - Archive Data Header Definition

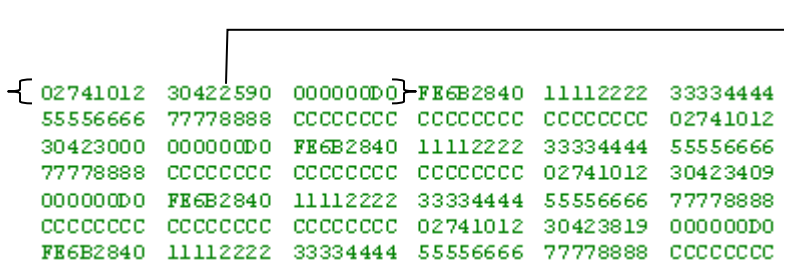
- Time Code Reader Error
- Time Code Flywheel Error
- Bit Sync Source (0 = Internal, 1=External)
- Bit Slip (1 = yes, 0 = no)
- Bit Sync Loop Lock
- Sub Frame Lock (2 = Lock, 1 = Check, 0 = Search)
- Minor Frame Lock (2 = Lock, 1 = Check, 0 = Search)
- Current Format # Indicator

9.4 Data Description

The Gryphon100 continuously packs the frame data into a file in 32 bit chunks. If a minor frame size (bits) is not divisible by 32. Then the end of the minor frame will be zero filled.

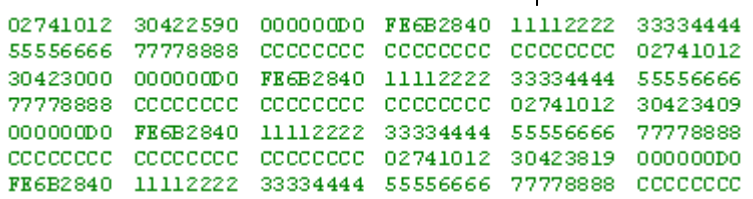
9.4.1 Archive Data 32 Bit Sync 16 Bit Data

Sync Pattern Size: 32 bits
Sync Pattern: FE6B2840
Minor Frames: 1
Words per Frame: 16



Header Information
Time = 274:10:12:30.422.590
Minor Frame Count = 0
Internal Bit Sync
No Bit Slips
Bit Sync Loop Lock
Sub Frame = Lock
Minor Frame = Lock
Current Format = 0

Figure 59 - Archive Data Header Example

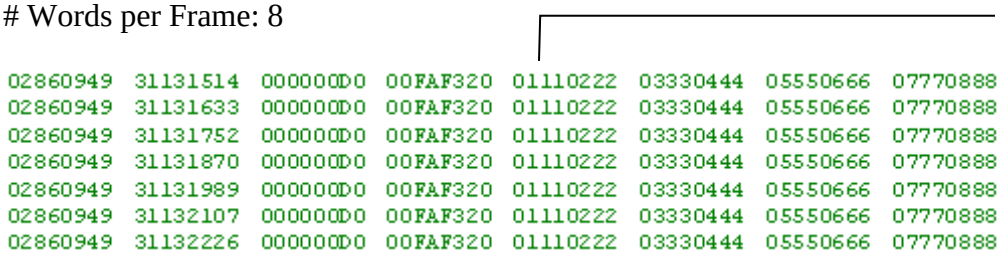


Data Information
Word 1 = 1111
Word 2 = 2222
Word 3 = 3333
Word 4 = 4444
Word 5 = 5555
Word 6 = 6666
Word 7 = 7777
Word 8 = 8888
Word 9 – 14 = CCCC

Figure 60 - Archive Data Example

9.4.2 Archive Data 24 Bit Sync 12 Bit Data

Sync Pattern Size: 24 bits
Sync Pattern: FAF320
Minor Frames: 1
Words per Frame: 8



Data Information In (Hexadecimal)
Word 1 = 0111
Word 2 = 0222
Word 3 = 0333
Word 4 = 0444
Word 5 = 0555
Word 6 = 0666
Word 7 = 0777
Word 8 = 0888

Figure 61 - 12 bit Archive example

Chapter 12 Pinout Map

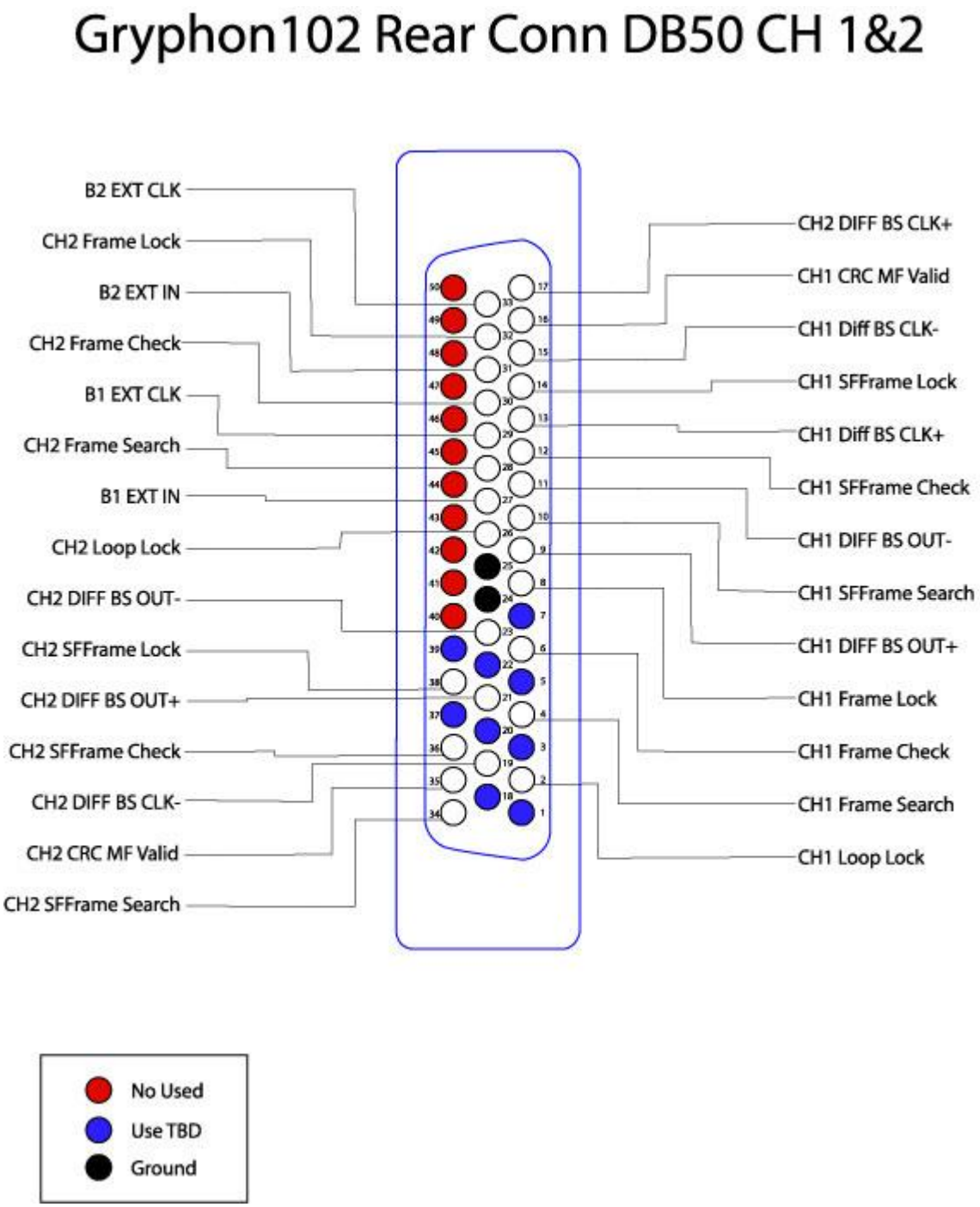


Figure 62 - Gryphon102 Rear Conn DB50 CH 1 & 2 Pin Layout

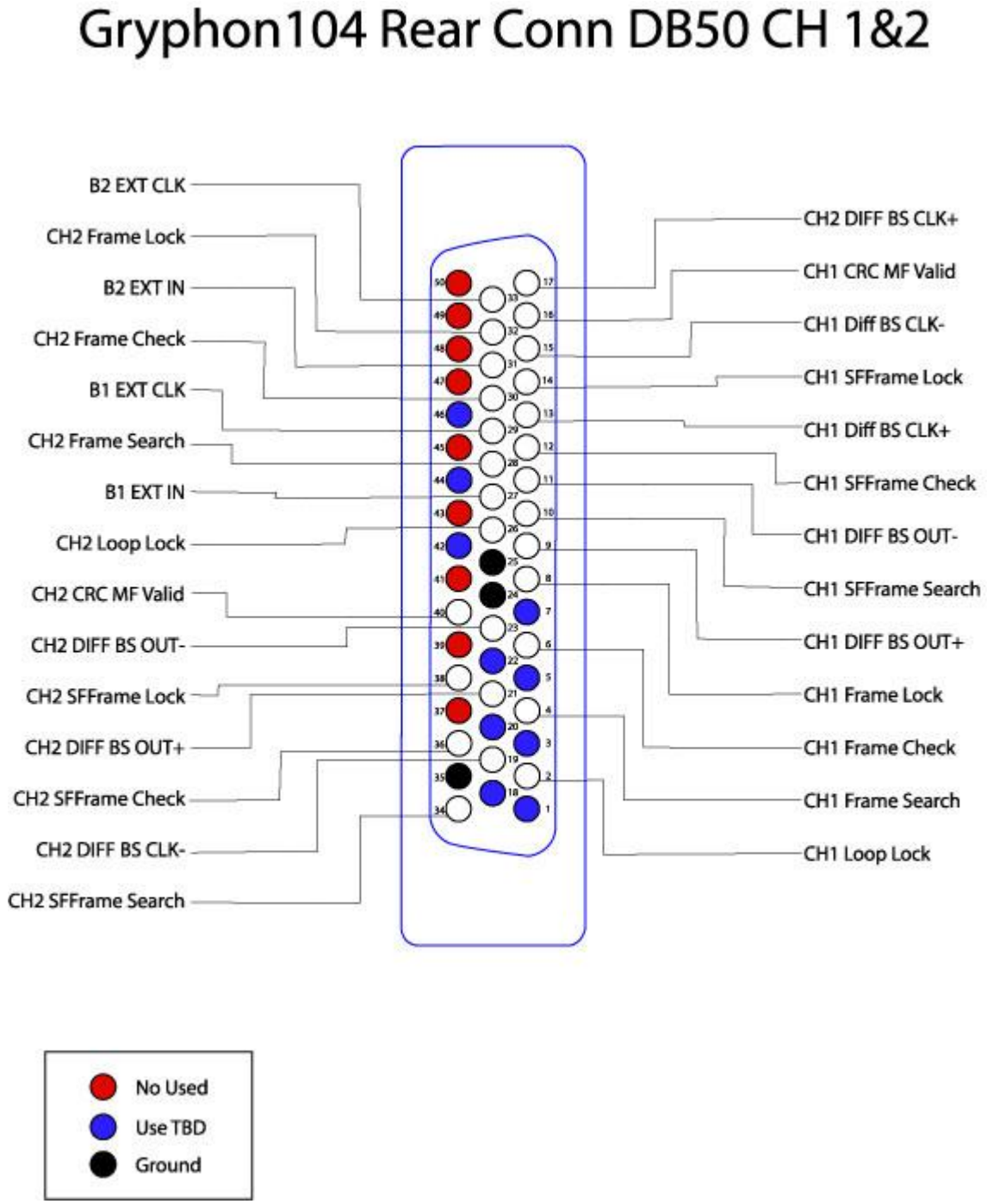


Figure 63 - Gryphon104 Rear Conn DB50 CH 1 & 2 Pin Layout

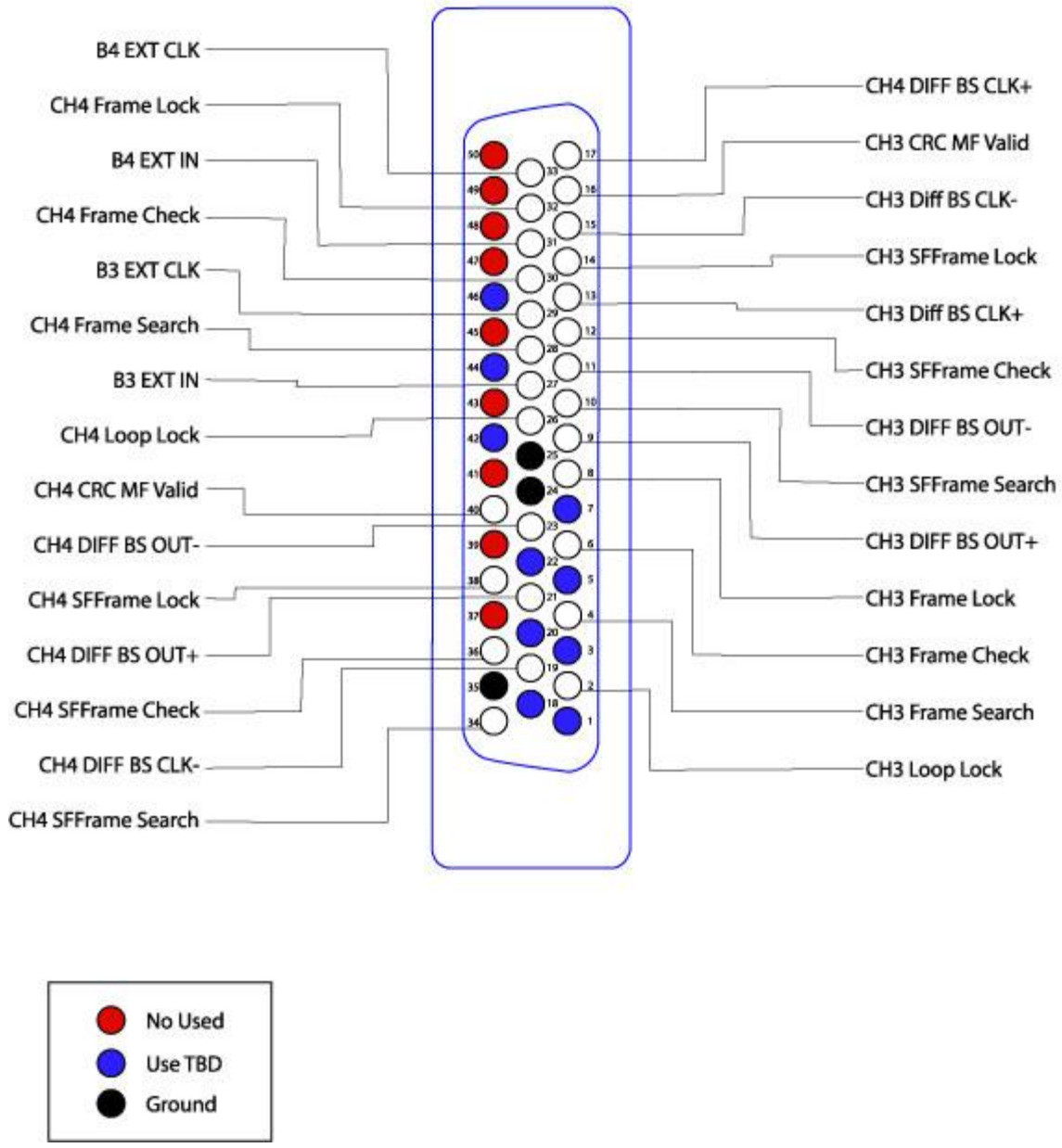


Figure 64 - Gryphon104 Rear Conn DB50 CH 3 & 4 Pin Layout

Chapter 13 FEC and Viterbi Theory

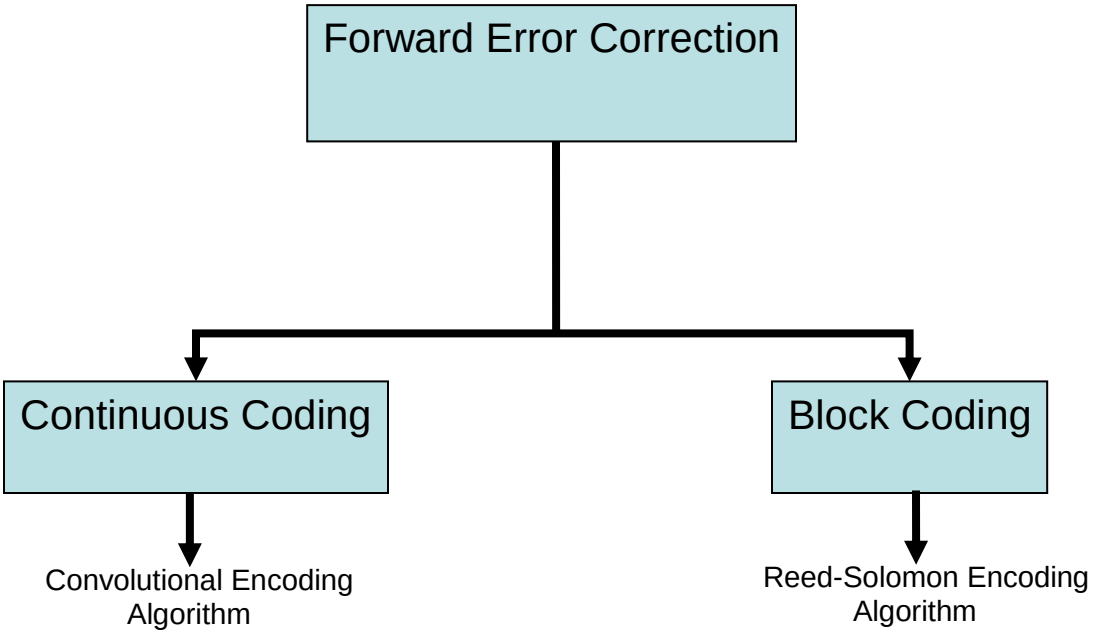


Figure 65 – Forward Error Correction Block Diagram

Figure 119 shows a diagram describing the algorithm choices to implement Forward Error Correction. Viterbi Decoding is the most common algorithm used in conjunction with a Convolutional Encoder and is the choice for the Ulyssix decoder.

- **Forward Error Correction (FEC)**
  - Forward error correction is a method that allows users to improve error control capabilities.
  - This is accomplished by transmitting redundant bits to the original data stream which can then be used to detect and correct errors.
  - Eliminates the need to resend data that usually results from transmission errors.
  - The error correcting ability is determined by the design of the error correcting code.

- **2 Most Common Categories of FEC**

  1.) Continuous Codes
  - Performs operations on bit or symbol streams of arbitrary length.
  - Commonly referred to as **Convolutional Coding**

  - Most common decoding method **Viterbi Decoding**

2.) Block Codes
  - Performs operations on fixed-size blocks or packets of symbols whose size is usually a function of a preset algorithm.
  - Most common type is **Reed-Solomon Coding**

- **Convolutional versus Block Encoding**
  - Soft-Decision Data permits Convolutionally Encoded System gain to degrade slowly as the error rate increases, whereas Block-Level codes only correct errors up to a point and the gain drops off rapidly afterwards.
  - Convolutional codes do not require block synchronization
  - Convolutional codes are decoded after an arbitrary length of data whereas block-level codes require the reception of an entire data block before decoding begins.

- **Convolutional Encoder Parameters**
- Commonly specified by three parameters:
  - n : number of output bits
  - k : number of input bits
  - m : number of memory registers
- Code Rate: k/n
  - Ratio describing the number of input to output bits
  - Also an indicator of code efficiency
  - Expressed as k/n
    - k ranges from 1 to 8, m from 2 to 10 and k/n from 1/8 to 7/8
- Constraint Length: K
  - Represents the number of bits in encoder memory
  - Directly affects the generation of output bits n
- Generator Polynomials: G1, G2
  - Used to choose which register bits are selected from registers
  - Number of polynomials is dependent on n

Viterbi Soft Bit Decision

Soft-Decision increases the Viterbi Decoder's ability to correctly decode an incoming data stream by quantizing a specified number of bits. The Ulyssix Viterbi Decoder uses a **seven** bit soft decision making. This means that for the rate ½ of each of the two encoded bits are now represented by 7 bits instead of one. When only a single bit is used for the two encoded bits this is called Hard Bit Decision. Since we are using seven bits, eight represents the maximum likely hood that binary a '1' was received whereas 0 represents the maximum likely hood that a binary '0' was received.